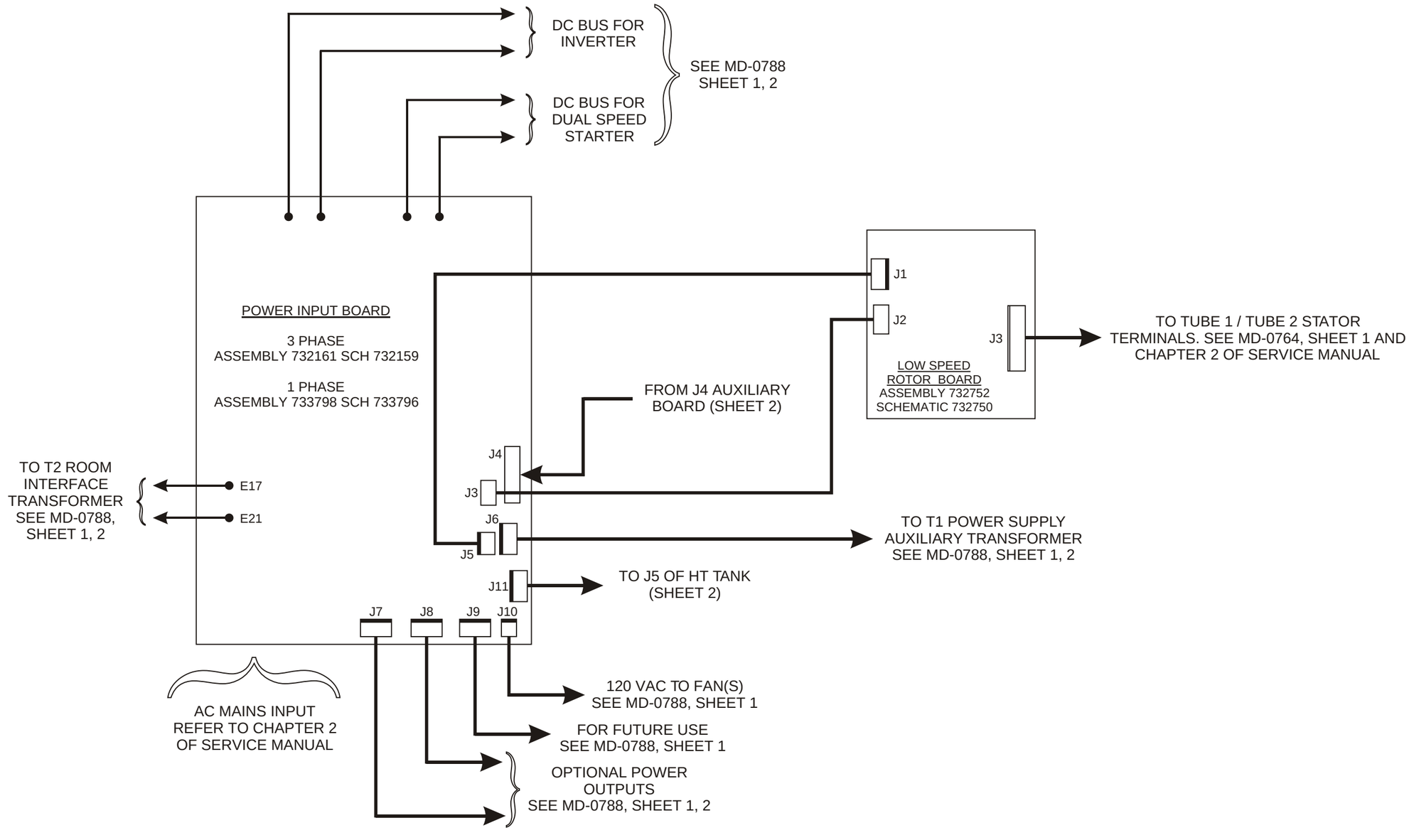

DRAWN G. SANWALD	DATE 02 MAR 2004	INTERCONNECT DIAGRAM (INDICO 100)
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DES.\MFG.\AUTH. L. FOSKIN	02 MAR 2004	MD-0843 REV H
		SHEET 1 OF 4

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FROM J1, OUTPUT CURRENT SENSE TRANSFORMER, ON RESONANT BOARD (SHEET 3)

J9 J13 J10 J11 J12

INVERTER DRIVE (SHEET 3)

FROM J10 GENERATOR CPU BOARD (SHEET 4)

J1

FROM J3 GENERATOR CPU BOARD (SHEET 4)

J2

CONTROL BOARD
ASSEMBLY 732816
SCHEMATIC 732814

J14 J15 J16

FROM INVERTER BOARD(S), SHEET 3

J3 J8 J4 J6 J7

J2 J1 J2 J1 J1 J5 J6

J1

FILAMENT SUPPLY BOARD
ASSEMBLY 731407
SCHEMATIC 731405

FILAMENT SUPPLY BOARD
ASSEMBLY 731407
SCHEMATIC 731405

SOME MODELS WILL HAVE ONLY ONE FILAMENT SUPPLY BOARD

AUXILIARY BOARD
ASSEMBLY 732221
SCHEMATIC 732219

J9

TB3

TB2

TO TUBE 1 / TUBE 2 STATOR TERMINALS. SEE MD-0765, SHEET 1 AND CHAPTER 2 OF SERVICE MANUAL

DUAL SPEED STARTER BOARD (OPTIONAL)
ASSEMBLY 728877
SCHEMATIC 728875

J4 J3 J5

J5 J5

J10 J2 J4 J7

HT TANK

X-RAY TUBE HOUSING GROUNDS

INTERNAL SYSTEM GROUNDS

FROM J11 POWER INPUT BOARD (SHEET 1)

FROM T1 POWER SUPPLY AUXILARY TRANSFORMER SEE MD-0788, SHEET 3

TO J4 POWER INPUT BOARD (SHEET 1)

TO K1 ON RESONANT BOARD (SHEET 3)

FROM THERMAL SWITCH ON INVERTER (SHEET 3). SEE MD-0787

NOT USED

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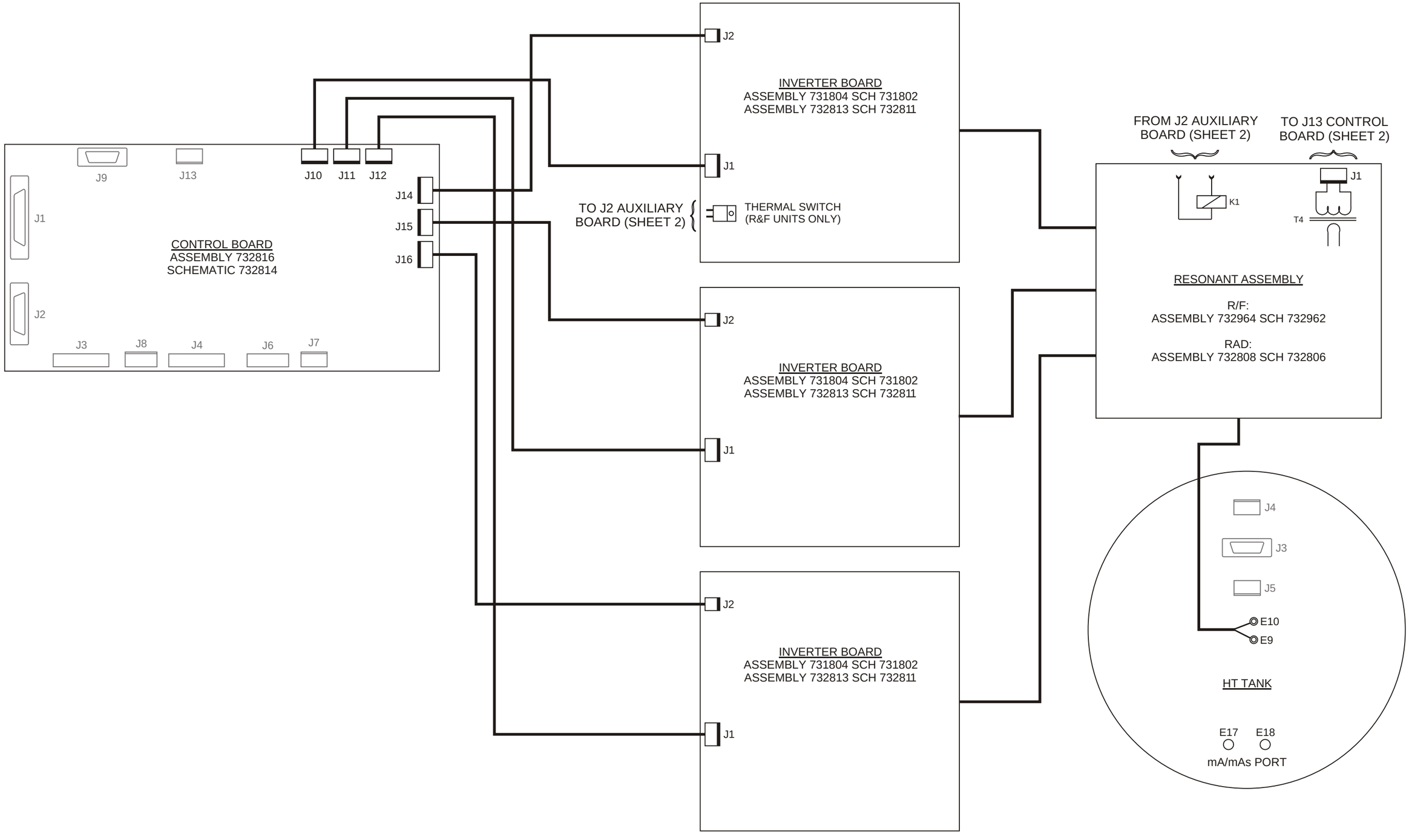

DEPENDING ON MODEL, ONE, TWO, OR
THREE INVERTER BOARDS WILL BE USED

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TO J2 CONTROL BOARD (SHEET 2)

TO J1 CONTROL BOARD (SHEET 2)

J3

J10

TO OPTIONAL REMOTE FLUORO CONTROL SEE MD-0766

J11

J2

GENERATOR CPU BOARD
ASSEMBLY 734573
SCHEMATIC 734571

SERIAL COMMUNICATIONS PORT

J1

J13

J15

J16

J7

J6

AEC BOARD (OPTIONAL)

ASSY 728399 SCH 728401
ASSY 733347 SCH 733345
ASSY 734614 SCH 734612
ASSY 734630 SCH 734628
ASSY 737992 SCH 737990
ASSY 737998 SCH 737996

REFER TO MD-0757 AND CHAPTER 3D OF SERVICE MANUAL

J5

TO DAP CHAMBERS. SEE MD-0828 AND CHAPTER 3F OF SERVICE MANUAL

J1 J2 J3

J4

DAP INTERFACE BOARD (OPTIONAL)
ASSEMBLY 735992
SCHEMATIC 735990

ACTIVE DOSE REDUCTION TANK (OPTIONAL)

J3

TO J15 GENERATOR INTERFACE BOARD

J10 J11 J12

J9

SEE NOTE 2

J8 *

* SEE NOTE 3

J6

J18

FOR FUTURE USE

SEE NOTE 1:

J4

J17

J7 *

J14

TO A^2EC^2. SEE MD-0757 SHEET 1

J16

J15

J13

J3

J5

J2

J1

GENERATOR INTERFACE BOARD
ASSEMBLY 732177
SCHEMATIC 732175

TB7 GND

TB8 24 VDC

TB9 110 VAC

TB10 220 VAC

ROOM INTERFACE BOARD
ASSEMBLY 733184
SCHEMATIC 733182

J2

J1

DIGITAL INTERFACE BOARD (OPTIONAL)

ASSY 733752 SCH 733750
ASSY 733947, 735921 SCH 733946
ASSY 735406 SCH 735404
ASSY 736153 SCH 736151
ASSY 736894 SCH 736892
ASSY 737950 SCH 737948

REFER TO MD-0767 AND DIGITAL IMAGING SUPPLEMENT IN FRONT OF SERVICE MANUAL

J1

FROM X-RAY TUBE THERMAL SWITCH. SEE MD-0787 AND CHAPTER 2 OF SERVICE MANUAL

FROM T2 ROOM INTERFACE TRANSFORMER. SEE MD-0788, SHEET 4

NOTE 1: J4 CONNECTS TO J5 ON THE 23 X 56 AND THE 31 X 42 CM CONSOLE, AND TO J2 ON THE TOUCH SCREEN CONSOLE. J16 CONNECTS TO J8 ON THE RAD-ONLY CONSOLE.

NOTE 2: J17 CONNECTS TO AN EXTERNAL EMERGENCY POWER-OFF SWITCH AND ALSO SUPPLIES POWER FOR AN INSTALLER-SUPPLIED POWER DISTRIBUTION RELAY. REFER TO MD-0788 SHEET 4, MD-0762 SHEET 1, AND TO CHAPTER 2 OF THE SERVICE MANUAL FOR DETAILS.

NOTE 3: J7 AND J8 ARE ABS INPUTS. REFER TO MD-0758 AND TO CHAPTER 3E OF THE SERVICE MANUAL FOR DETAILS.

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		SHEET 4 OF 4

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REFER TO PAGE 5 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY HEXAGONAL SYMBOL: ⬡

3 PHASE AC MAINS INPUT

PHASE 1 — F5B
PHASE 2 — F5A
PHASE 3 — F5C
NEUTRAL
GROUND

K5 — D1 — R18, R19 — R20 — DC BUS OUT — E23 — E11

3 PHASE INDICO 100 GENERATORS USE ONE, TWO, OR THREE INVERTER BOARDS DEPENDING ON GENERATOR OUTPUT POWER

E1 + / E2 - INVERTER BOARD (×3)

E15 — E8 — R16, R17

E9 — F2 — + — E10 — F1 — 560 VDC ** — -
DUAL SPEED STARTER BOARD

DUAL SPEED STARTER IS OPTIONAL. LOW SPEED STARTER IS STANDARD IN INDICO 100 GENERATORS

K1 — F2 — F1

DC BUS CHARGED SENSING CIRCUIT (R5-R8, D3)

DC BUS DISCHARGE CIRCUIT (Q1, D10)

F7 — +12V — RN2 — U1 — U2 — DS1 — DC BUS OK — +12VDC OK — DS2

BUZZER ANNUNCIATOR (R33-R35, R46, R47, Q3, Q4) — LS1

T1 — 380/400/480 VAC * — 240 VAC — N/C — 208 VAC — 120 VAC — 94 VAC — 73 VAC — 52 VAC — RETURN

J6-1 — J6-5 — J6-6 — J6-7

CONTINUED ON PAGE 3

J1-1 — F1 — 120 / 240 VAC
J1-3 — F2 — 52 / 73 / 94 VAC
J1-4 — F3 — COMMON

J5-3 — J5-4

J3-3 — J3-4 — J3-2 — J2-3 — J2-4 — J2-2 — TP4 — TP1

J3-9 — J2-9 — REFER TO MD-0764
LOW SPEED STARTER BOARD

J10-3 — J10-1 — J11-4 — J11-6

COOLING FAN(S) USED ON SOME MODELS. DEPENDING ON THE APPLICATION, ONE, TWO, OR THREE FANS MAY BE USED

K4 — F6 — K3 — F8 — F2 — THREE FAN UNITS ONLY

J5-4 — J5-6 — TUBE 1 /TUBE 2 SOLENOID (TWO TUBE HT TANKS ONLY)
H.T. TANK

J8-3 — J8-1 — J7-1 — J7-3 — J7-5 — F3

OPTIONAL 400/480*** VAC
*** 480 VAC GENERATORS
230/277*** VAC
NEUTRAL
GROUND
OPTIONAL
ROOM INTERFACE CHASSIS

J9-5 — J9-4 — J9-2 — J9-1

E14 — E18

ROOM POWER KIT OPTION
REFER TO SEPARATE SUPPLEMENT, IF APPLICABLE

FOR FUTURE USE

E21 — E17

3 PHASE POWER INPUT BOARD (REFER TO PAGE 2 FOR 1 PHASE POWER INPUT BOARD)

* T2 (SHOWN TAPPED FOR 400 VAC MAINS)

F4 — 240V — 200V — 180V — 0V — 240V — 200V — 0V

CONTINUED ON PAGE 4

*** JW1 fitted on units where fans must run continuously

JW3 — JUMPER NOT FITTED (ALL MODELS) — SOFT START OK PROTECTION CIRCUIT (U1C, Q7, ETC) — K1 — D3 S.S. OK — +12V — R48 — J4-10 — J4-8

JW2 — JUMPER NOT FITTED (ALL MODELS) — SOFT START DRIVER CIRCUIT (U3B, Q6, ETC) — D2 — R31 — CNCTR CLOSED — J4-13

SOFT START FAULT SIGNAL TO AUXILIARY BOARD, PAGE 3

R1, R2 — K1 — J4-1 — J4-4 — J4-3 — J4-14 — J4-15 — J4-16 — J4-18 — J4-17

TUBE 1 / TUBE 2 SELECT COMMAND TO MD-0787

RN1 — RN2 — DS4 — D4 — J2-1 P2-1 — J2-2 P2-2 — K5 — D8 — K2 — DS6 — D5 — K1 — DS7 — R32 — U3 — Q2

TP1

FLUORO FAN TIMER / DRIVER CIRCUIT (U11, Q9, ETC) — R72 — D37 FLUORO FAN ON — R&F GENERATORS ONLY — *** JW1 — D6 — K4 — DS5

J5-6 — J5-7 — J5-3 — J5-4 — J1-6 — J1-5 — J1-3

AUXILIARY BOARD

FROM PAGE 3

---

* T1 AND T2 MUST BE TAPPED IN ACCORDANCE WITH THE NOMINAL AC MAINS VOLTAGE. REFER TO CHAPTER 2 OF THE GENERATOR SERVICE MANUAL.

** THIS VOLTAGE IS APPROXIMATELY 560 VDC FOR 400 V GENERATORS, AND APPROXIMATELY 680 VDC FOR 480 V GENERATORS

DRAWN G. SANWALD	DATE 10 MAR 2000	**DC BUS & POWER DISTRIBUTION**
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		SHEET 1 OF 6

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1 PHASE AC MAINS INPUT

LINE 1

LINE 2

GROUND

F5A

F5B

K5

E33

E34

230 VAC

MAINS RECTIFIER

BUS CAPACITORS

VOLTAGE DOUBLER CIRCUIT

650 VDC OUT

DC BUS ASSEMBLY

SINGLE PHASE INDICO 100 GENERATORS USE ONE OR TWO INVERTER MODULES DEPENDING ON GENERATOR OUTPUT POWER

E1 +

INVERTER BOARD

E2 -

E1 +

INVERTER BOARD

E2 -

ROOM POWER KIT OPTION
REFER TO SEPARATE SUPPLEMENT, IF APPLICABLE

R10

R11

K1

F2

F1

P1-4

P1-1

J12-4

J12-1

DC BUS CHARGED SENSING CIRCUIT (R6-R8, R16-R21, D3, ETC)

NO CONNECTION

J6-1

380/400/480 VAC TAPS

*T1

240 VAC

208 VAC

120 VAC

94 VAC

73 VAC

52 VAC

RETURN

J6-3

J6-5

J6-6

J6-7

F1

CONTINUED ON PAGE 3

AUXILIARY BOARD
REFER TO PAGE 1

1

J4-10

J4-8

J4-13

J4-2

J4-1

J4-4

J4-3

J4-14

J4-15

J4-16

J4-18

J4-17

J4-5

6

+12V

R36

DS4

D4

J2-1 P2-1

J2-2 P2-2

K5

U1

DS1

DC BUS OK

K2

R39

D8

DS6

R34

R33

R29

U2

Q1

R35

D5

K1

R38

DS7

D7

K3

R37

D6

K4

DS5

R12

DS2

+12VDC OK

F4

R40

DS3

J5-3

J5-4

J3-3

J3-4

J3-2

J3-9

LOW SPEED STARTER BOARD
REFER TO PAGE 1

J10-3

J10-1

K4

K3

COOLING FAN(S) USED ON SOME MODELS. DEPENDING ON THE APPLICATION, ONE, TWO, OR THREE FANS MAY BE USED

J11-4

J11-6

H.T. TANK
REFER TO PAGE 1

J8-3

J8-1

J7-1

J7-3

J7-5

F3

OPTIONAL 230 VAC

230 VAC

GROUND

OPTIONAL

ROOM INTERFACE CHASSIS

E21

E17

1 PHASE POWER INPUT BOARD

* T2 (SHOWN TAPPED FOR 240 VAC MAINS)

F4

240V

200V

180V

0V

240V

200V

0V

E14

E18

ROOM POWER KIT OPTION
REFER TO SEPARATE SUPPLEMENT, IF APPLICABLE

CONTINUED ON PAGE 4

* T1 / T2 MUST BE TAPPED IN ACCORDANCE WITH THE NOMINAL AC MAINS VOLTAGE. REFER TO CHAPTER 2 OF THE GENERATOR SERVICE MANUAL.

DRAWN G. SANWALD	DATE 10 MAR 2000	DC BUS & POWER DISTRIBUTION
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		SHEET 2 OF 6

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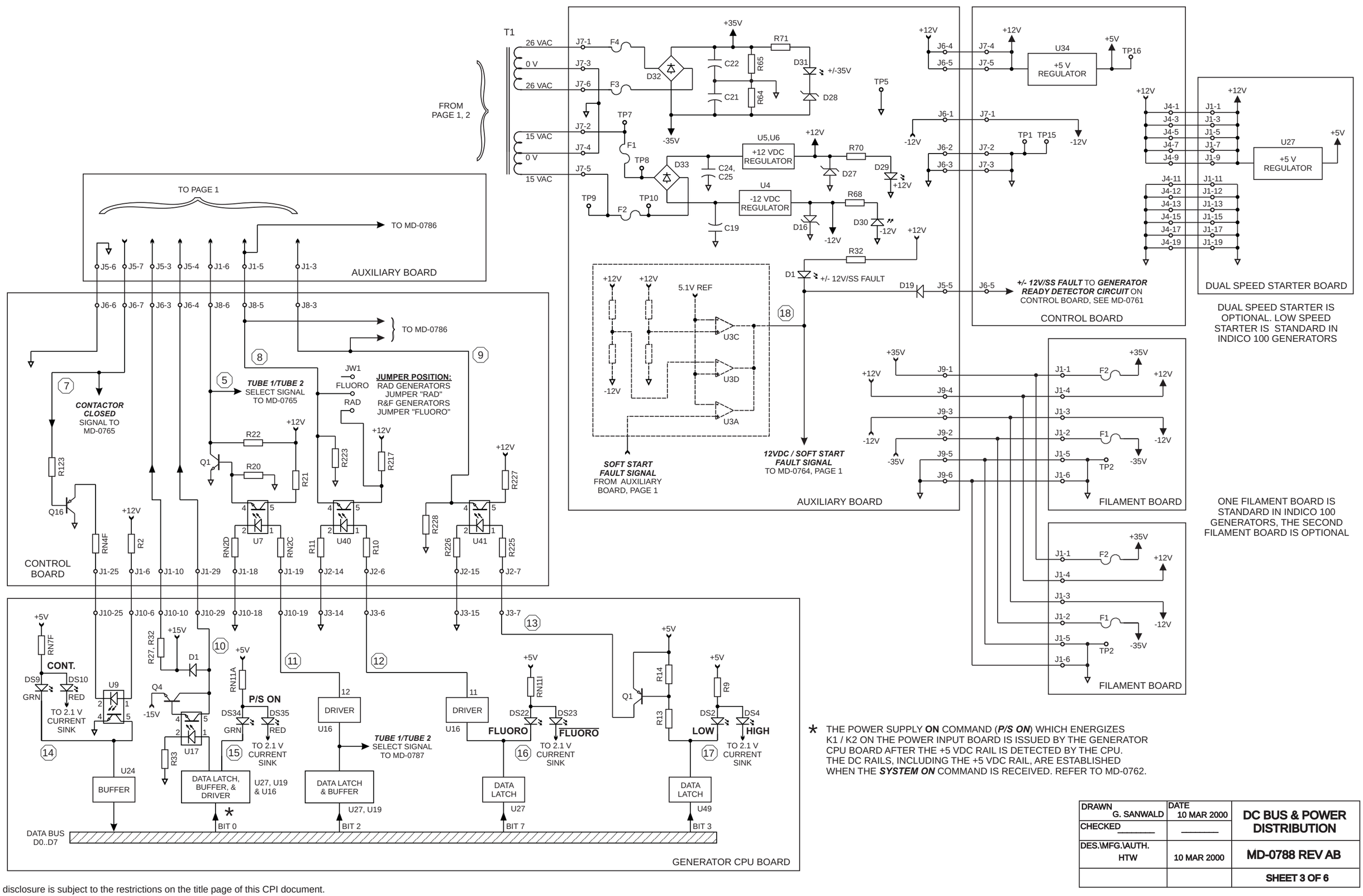

* THE POWER SUPPLY **ON** COMMAND (***P/S ON***) WHICH ENERGIZES K1 / K2 ON THE POWER INPUT BOARD IS ISSUED BY THE GENERATOR CPU BOARD AFTER THE +5 VDC RAIL IS DETECTED BY THE CPU. THE DC RAILS, INCLUDING THE +5 VDC RAIL, ARE ESTABLISHED WHEN THE ***SYSTEM ON*** COMMAND IS RECEIVED. REFER TO MD-0762.

DRAWN G. SANWALD	DATE 10 MAR 2000	**DC BUS & POWER DISTRIBUTION**
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		SHEET 3 OF 6

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FROM PAGE 1, 2

T2
18 VAC
0 V
18 VAC
0 V
18 VAC
110 VAC
220 VAC
J1-2
J1-1
J1-3
J1-4
J1-5
J1-7
J1-9
F5
F3
F4
F2
F1
D3
D1
C10
C16
K2
K1
K3
24 VDC RETURN
24 VDC
+24V
TP13
R81
U5
+15 V REGULATOR
+15V
R1
TP1
+5 / +16VDC POWER SUPPLY CIRCUIT (U47, Q4, T1, D17, D18, ETC.)
+5V
R3
TP3
F6
U3
+12 V REGULATOR
TP2
R2
+12V
U2
-12 V REGULATOR
R6
TP7
-12V
-24V
R5
TP6
U4
-15 V REGULATOR
R4
TP5
-15V
U40
ZERO CROSS DETECTOR
R78
D15
LINE SYNC
TO MD-0767
110 VAC
220 VAC

K1
K2
K3
REFER TO ***SYSTEM ON***, MD-0762

TO COIL OF POWER DISTRIBUTION RELAY (CUSTOMER SUPPLIED) MAXIMUM 100 MA
+24V
J17-3
J17-4

GENERATOR INTERFACE BOARD
J13-9
J13-21
J13-23
J13-11
J13-13
J13-17
J13-15
+5V
+15V
+24V
-15V

THE DIGITAL I/O BOARD IS OPTIONAL WITH R&F GENERATORS

REFER TO MD-0767 (DIGITAL INTERFACE) FOR PINOUTS OF THE DC RAIL CONNECTIONS SHOWN TO THE RIGHT OF THIS TEXT

DIGITAL I/O BOARD

J4-12
J4-14
J4-13
J4-15
J16-3
J16-8
J5-12
J5-14
J5-13
J5-15
REFER TO ***SYSTEM ON***, MD-0762
TP11
TP7
F1
+ 5V, + 3.3V, +1.2V AND - 15V POWER SUPPLY CIRCUITS (U9, U10, U11, D1-D6, L1, ETC.)
+5V
TP8
+3.3V
TP12
TP2
+1.2V
TP10
-15V
TO RAD-ONLY CONSOLE (PAGE 5)
+5V
TP9
19
300 VAC BACKLIGHT POWER SUPPLY (Q2, Q3, T1, C61, ETC)
J10-1
J10-4
FLUORESCENT LAMP
LCD DISPLAY ASSEMBLY

CONSOLE BOARD (31 X 42 CM CONSOLE)

CONSOLE BOARD & LCD DISPLAY ASSEMBLY SHOWN WITHIN DASHED LINES USED ON 31 X 42 CM CONSOLE ONLY. REFER TO PAGE 5 FOR 23 X 56 CM CONSOLE AND FOR RAD-ONLY CONSOLE.

220 VAC
110 VAC
+24V
J2-1
J2-3
J2-6
J2-7
J2-8
J2-9
J1-1
J1-3
J1-6
J1-7
J1-8
J1-9
220 VAC
110 VAC
+24VDC
R7
DS1
POWER ON

ROOM INTERFACE BOARD

+12V
+24V
J10-13
J10-19
J10-11
J10-16
J10-17
-12V
-24V
REFER TO MD-0757 (AEC) FOR PINOUTS OF THE DC RAIL CONNECTIONS ON THE AEC BOARD

AEC BOARD

+15V
+12V
+5V
J3-3
J3-6
J3-1
J3-8
J3-5
-12V
-15V
J13-3
J13-6
J13-1
J13-8
J13-5
TP17
R77
TP19
R85
TP16
R75
R89
TP20
R80
TP18
TP4
J3-2
J3-4
J3-7
J13-2
J13-4
J13-7
TP21
R78
R86
R76
DS36
DS38
DS33
DS37
DS39
R81
R90
J11-1
J11-5
TO REMOTE FLUORO CONTROL, PAGE 5

GENERATOR CPU BOARD

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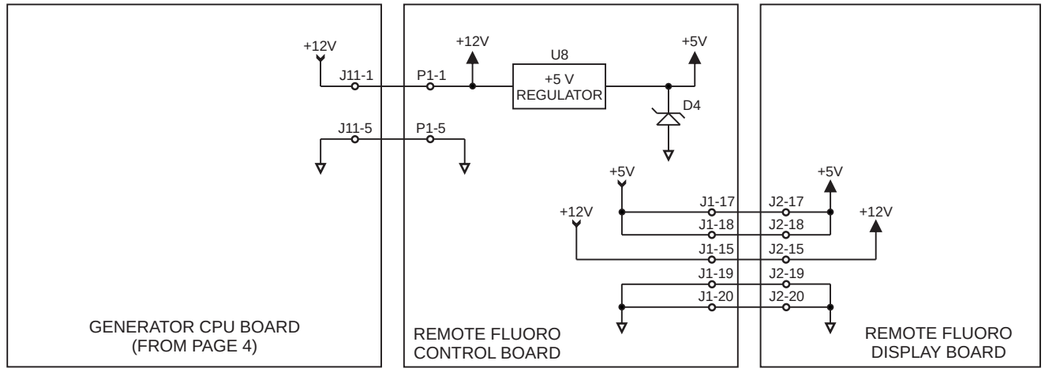
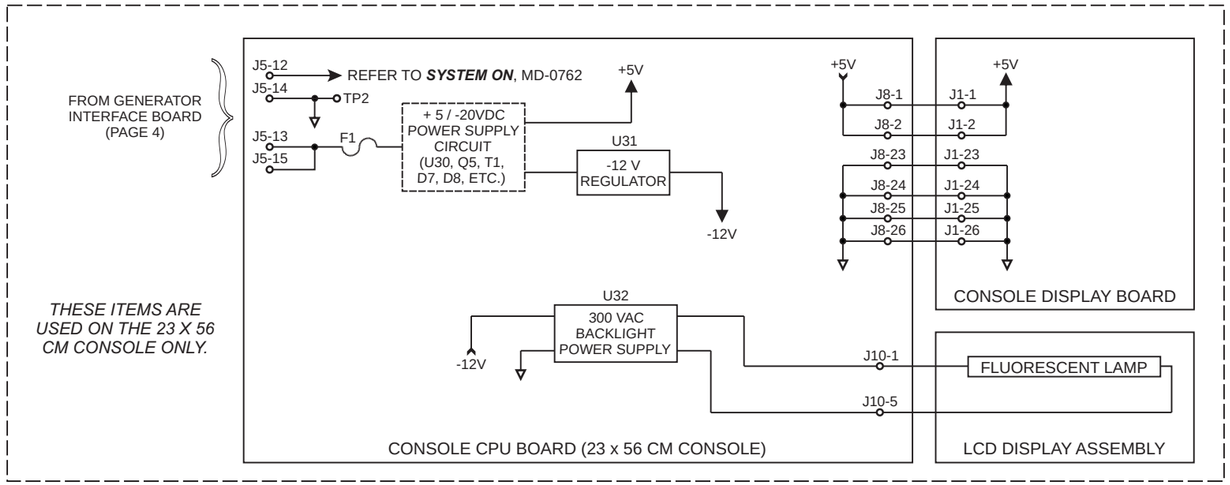
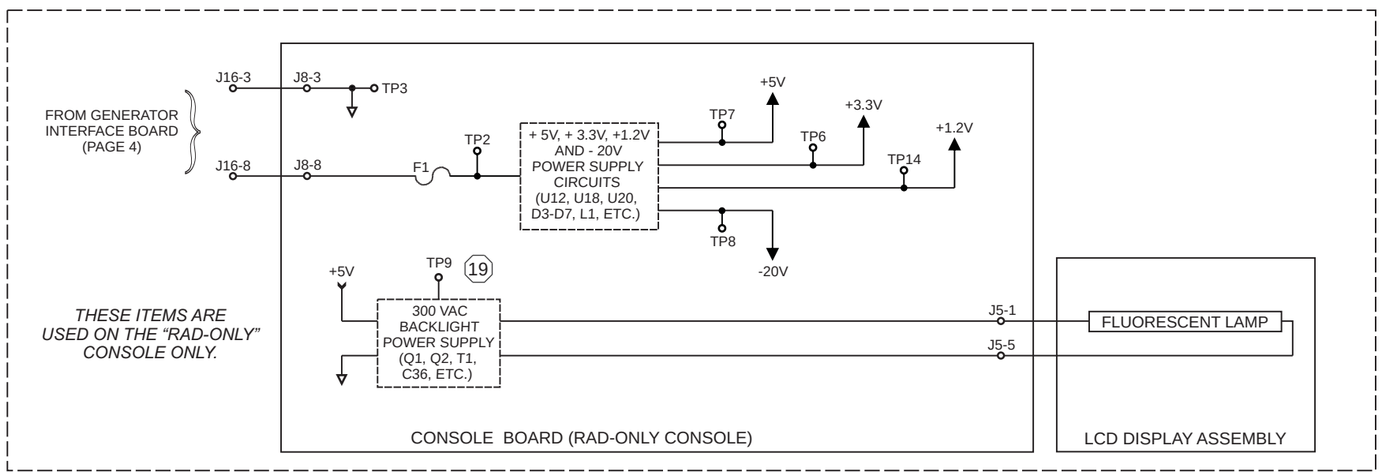


REMOTE FLUORO CONTROL OPTIONAL WITH
INDICO 100 R&F GENERATORS





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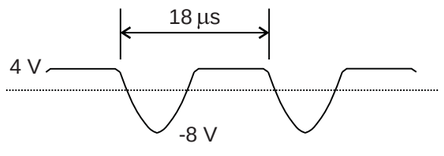
NOTE REFERENCE	REMARKS
1	THIS VOLTAGE WILL BE APPROXIMATELY 0 VDC WHEN THE DC BUS CAPACITORS ARE NOT CHARGED. THIS WILL RISE TO APPROXIMATELY 6 VDC WHEN THE DC BUS CAPACITORS ARE FULLY CHARGED.
2	THE DC BUS CAPACITORS MUST CHARGE WITHIN APPROXIMATELY 0.25 SECONDS OF THE GENERATOR BEING SWITCHED ON. IF THE DC BUS CAPACITORS DO NOT CHARGE NORMALLY, THE ***SOFT START OK PROTECTION CIRCUIT*** ENERGIZES RELAY K1 (SEE # 4) AND INHIBITS OPERATION OF THE ***SOFT START DRIVER CIRCUIT*** (SEE # 3).
3	"LOW" (APPROXIMATELY 0 VDC) COMMANDS THE MAIN CONTACTOR K5 ON THE POWER INPUT BOARD TO CLOSE. "HIGH" (APPROXIMATELY 12 VDC) = CONTACTOR OPEN. THIS OUPUT WILL NOT SWITCH "LOW" IF THE DC BUS CAPACITORS ARE NOT CHARGED (SEE # 1 & 2).
4	K1 REMAINS DE-ENERGIZED (CONTACTS AS SHOWN) IF NO SOFT-START FAULT IS DETECTED. THEREFORE, K1 **AND** K2 ON THE POWER INPUT BOARD WILL ENERGIZE WHEN THE GENERATOR IS SWITCHED ON. A SOFT-START FAULT ENERGIZES K1 ON THE AUXILIARY BOARD, DE-ENERGIZING K1 ON THE POWER INPUT BOARD. THIS WILL INHIBIT FURTHER DC BUS CHARGING.
5	"LOW" (APPROXIMATELY 0 VDC) = TUBE 2 SELECTED, "HIGH" (APPROXIMATELY 12 VDC) = TUBE 1 SELECTED.
6	"LOW" (APPROXIMATELY 0 VDC) = FLUORO FAN(S) ON, "HIGH" (APPROXIMATELY 12 VDC) = FLUORO FAN(S) OFF. FAN(S) ARE SWITCHED ON DURING PULSED OR CONTINUOUS FLUORO OPERATION, AND REMAIN ON FOR APPROXIMATELY 20 MINUTES AFTER SWITCHING TO RAD MODE.
7	"LOW" INDICATES ***CONTACTOR CLOSED*** (SEE # 3). THE ***CONTACTOR CLOSED*** SIGNAL OCCURS APPROXIMATELY 10 SECONDS AFTER INITIAL GENERATOR TURN-ON, ASSUMING NORMAL DC BUS CHARGING.
8	"HIGH" (APPROXIMATELY 12 VDC) = RAD / PULSED FLUORO MODE. "LOW" (APPROXIMATELY 0 VDC) = CONTINUOUS FLUORO MODE. USED ON R&F GENERATORS ONLY.
9	"HIGH" (APPROXIMATELY 12 VDC) = PULSED FLUORO / LOW POWER MODE. "LOW" (APPROXIMATELY 0 VDC) = HIGH POWER RAD MODE. NOT USED ON ALL MODELS, REFER TO MD-0786 FOR DETAILS.
10	24 VDC (APPROXIMATELY) ENERGIZES K1 AND / OR K2 ON THE POWER INPUT BOARD, INITIATING THE POWER-ON SEQUENCE. SEE # 4.
11	"HIGH" (APPROXIMATELY 5 VDC) = TUBE 2 SELECTED. "LOW" (APPROXIMATELY 0 VDC) = TUBE 1 SELECTED.
12	"HIGH" (APPROXIMATELY 5 VDC) = RAD / PULSED FLUORO MODE. "LOW" (APPROXIMATELY 0 VDC) = CONTINUOUS FLUORO MODE. USED ON R&F GENERATORS ONLY.
13	"HIGH" (APPROXIMATELY 5 VDC) = PULSED FLUORO / LOW POWER MODE. "LOW" (APPROXIMATELY 0 VDC) = HIGH POWER RAD MODE. NOT USED ON ALL MODELS, REFER TO MD-0786 FOR DETAILS.
14	DS9 LIT = CONTACTOR CLOSED, DS10 LIT = CONTACTOR NOT CLOSED.
15	DS34 LIT = GENERATOR **ON** COMMAND ISSUED (CONSOLE PASSED ALL SELF TESTS). DS35 LIT = GENERATOR **ON** COMMAND NOT ISSUED (DURING CONSOLE SELF TESTS, OR IF SELF TESTS FAILED).
16	DS22 LIT = FLUORO SELECTED, DS23 LIT = RAD SELECTED.
17	DS2 LIT = PULSED FLUORO / LOW POWER MODE. DS4 LIT = HIGH POWER RAD MODE. SEE # 13.
18	D1 LIT INDICATES + OR - 12 VDC FAULT, OR SOFT START FAULT.
19	THE VOLTAGE WAVEFORM AT THIS TEST POINT IS DEPICTED IN FIGURE 1 BELOW.

FIGURE 1



DRAWN G. SANWALD	DATE 10 MAR 2000	DC BUS & POWER DISTRIBUTION
CHECKED _____	_____	
DES.\MFG.\AUTH. HTW	10 MAR 2000	MD-0788 REV AB
		SHEET 6 OF 6

Use and disclosure is subject to the restrictions on the title page of this CPI document.

T2
F5
D3
24 VDC RETURN
+ 24 VDC
24 VDC SUPPLY FOR SYSTEM ON/OFF. SEE MD-0788, PAGE 4
J17-1
J17-2
*
Q1
Q2
Q3
LOCKOUT
NORMAL
S3
R15
D4
D16
K3
K2
K1
REFER TO ***DC BUS & POWER DISTRIBUTION,*** MD-0788, PAGE 4
S1 OFF
S2 ON
R13
DS1
3
JW1
3
2
1
JUMPER POSITION:
TO ENERGIZE K1 ONLY WHEN THE CONSOLE IS SWITCHED ON
JUMPER JW1 PINS 1-2
TO ENERGIZE K1 AT ALL TIMES THAT THE GENERATOR AC MAINS IS ON
JUMPER JW1 PINS 2-3
(K1 SWITCHES THE 110 & 220 VAC SUPPLIES TO THE ROOM INTERFACE BOARD)

R & F MEMBRANE CONSOLE
ON
OFF
P1-3 J3-3 J5-10 J4-10 1
P1-2 J3-2 J5-11 J4-11 2
P1-1 J3-1 J5-12 J4-12
KEYBOARD ASSEMBLY
CONSOLE BOARD

RAD-ONLY CONSOLE
ON
OFF
P1-15 J7-15 J8-6 J16-6
P1-16 J7-16 J8-7 J16-7
P1-17 J7-17 J8-3 J16-3
KEYBOARD ASSEMBLY
CONSOLE BOARD

TOUCH SCREEN CONSOLE
DS1
J1-1 J16-1 R154
J1-3 J16-3
J1-4 J16-4 J28-10 J4-10
OFF SW1
ON SW2
J1-5 J16-5 J28-11 J4-11
J1-6 J16-6 J28-12 J4-12
FRONT PANEL BOARD
TOUCH SCREEN BOARD

GENERATOR INTERFACE BOARD

USE DRAWING ***DC BUS & POWER DISTRIBUTION,*** MD-0788, IN CONJUNCTION WITH THIS DOCUMENT

* TO CONNECT AN EMERGENCY-OFF SWITCH, REMOVE JUMPER FROM J17-1 TO J17-2. THEN CONNECT THE EMERGENCY OFF SWITCH TO J17-1 AND J17-2.

DRAWN G. SANWALD	DATE 02 JUN 2000	**SYSTEM ON**
CHECKED _____	_____	
DES.\MFG.\AUTH. L. FOSKIN	02 JUN 2000	**MD-0762 REV H**
		SHEET 1 OF 2

Use and disclosure is subject to the restrictions on the title page of this CPI document.

NOTE REFERENCE	REMARKS
1	MOMENTARILY PRESSING ***ON*** CONNECTS THIS LINE TO “24 VDC RETURN”. THIS LATCHES RELAY DRIVERS ON THE GENERATOR INTERFACE BOARD, ENERGIZING K2 AND K3, AND POSSIBLY K1 (DEPENDING ON JW1 SETTING). SEE NOTE ADJACENT TO JW1 ON THIS DOCUMENT.
2	MOMENTARILY PRESSING ***OFF*** CONNECTS THIS LINE TO “24 VDC RETURN”. THIS UNLATCHES RELAY DRIVERS ON THE GENERATOR INTERFACE BOARD, DE-ENERGIZING K2 AND K3, AND POSSIBLY K1 (DEPENDING ON JW1 SETTING).
3	DS1 LIT INDICATES THE PRESENCE OF THE 24 VDC SUPPLY SHOWN. THIS 24 VDC SUPPLY WILL BE PRESENT IF THE GENERATOR IS CONNECTED TO A LIVE AC MAINS SUPPLY.

DRAWN G. SANWALD	DATE 02 JUN 2000	SYSTEM ON
CHECKED _____	_____	
DES.\MFG.\AUTH. L. FOSKIN	02 JUN 2000	MD-0762 REV H
		SHEET 2 OF 2

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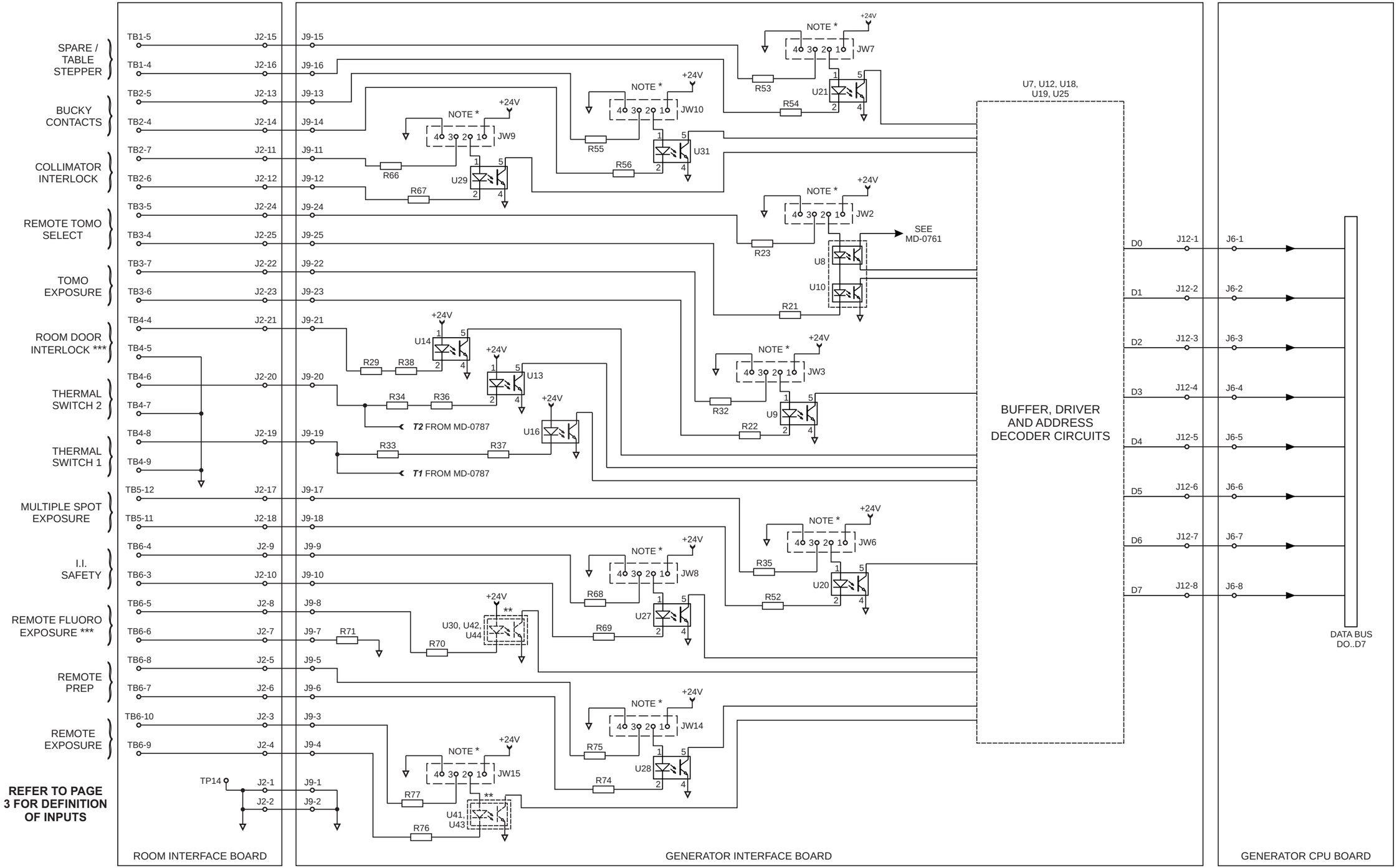

THIS PAGE SHOWS THE ROOM INTERFACE INPUTS. ROOM INTERFACE OUTPUTS ARE SHOWN ON PAGE 2

** ADDITIONAL CIRCUITS ARE USED IN THE AREAS INDICATED **. THESE CIRCUITS ARE NOT RELEVANT TO THIS ROOM INTERFACE DIAGRAM, HOWEVER, THEY ARE PART OF THE X-RAY EXPOSURE FUNCTION AND ARE SHOWN ON MD-0761

*** REFER TO “ROOM DOOR INTERLOCKS” ON SHEEET 3.

* 24 VDC EXTERNAL INPUT POSITION FOR JW2, JW3, JW6, JW7, JW8, JW9, JW10, JW14, JW15 SHOWN. JUMPER CONNECTS PINS 2-3; 24 VDC APPLIED EXTERNALLY ACTIVATES THE INPUT(S) BY ENERGIZING THE APPROPRIATE OPTO-COUPLER.

* DRY CONTACT INPUT POSITION FOR JW2, JW3, JW6, JW7, JW8, JW9, JW10, JW14, JW15 SHOWN. JUMPER CONNECTS PINS 1-2 AND 3-4; AN EXTERNAL DRY CONTACT CLOSURE ACTIVATES THE INPUT(S) BY ENERGIZING THE APPROPRIATE OPTO-COUPLER.

DRAWN G. SANWALD	DATE 13 APR 2000	ROOM INTERFACE
CHECKED S. BLAKE	14 APR 2000	
DES.\MFG.\AUTH. L. FOSKIN	13 APR 2000	MD-0763 REV K
		SHEET 1 OF 3

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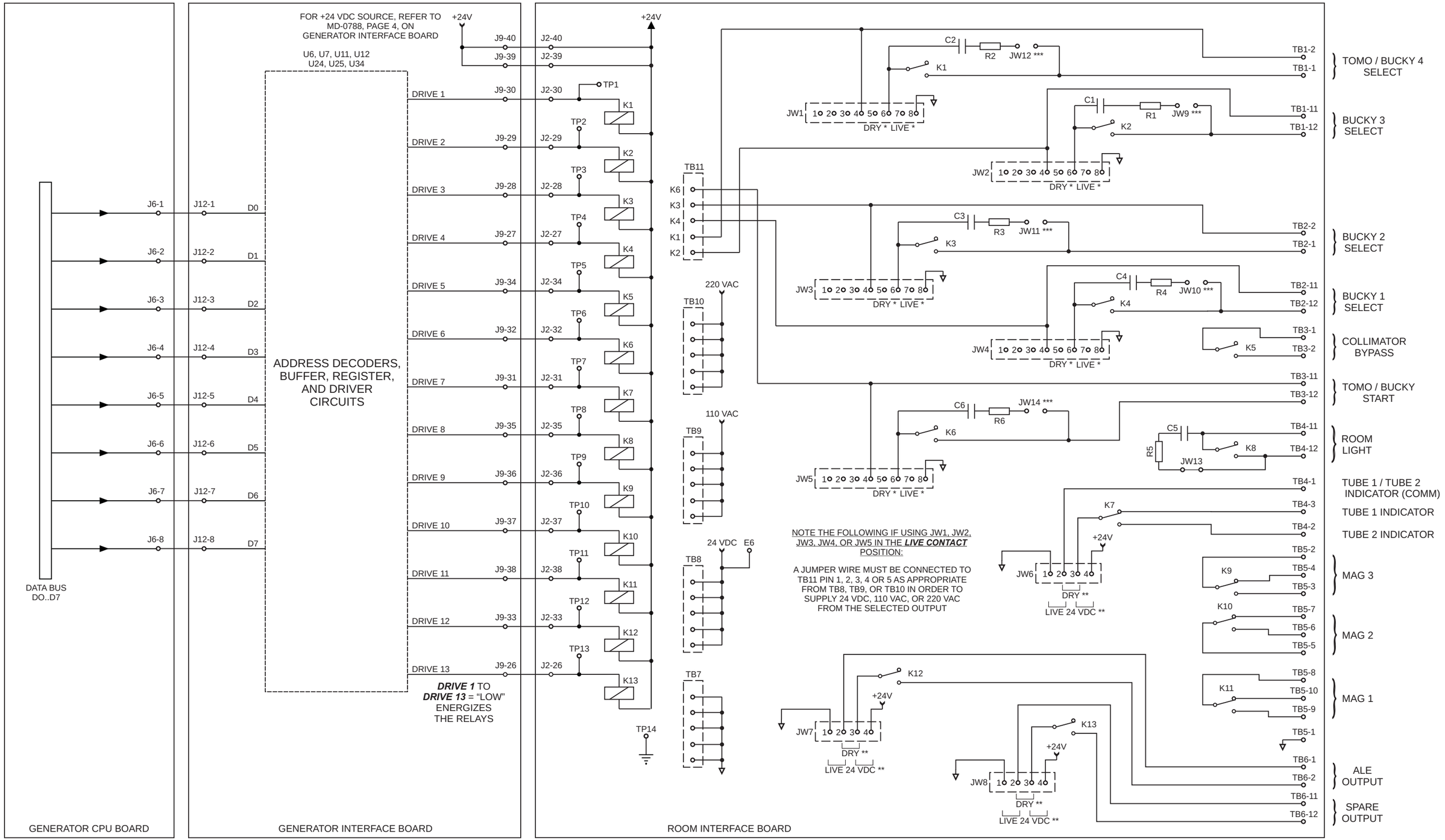
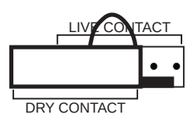
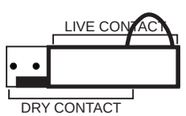


THIS PAGE SHOWS THE ROOM INTERFACE OUTPUTS. ROOM INTERFACE INPUTS ARE SHOWN ON PAGE 1

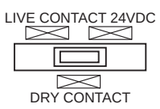
Use and disclosure is subject to the restrictions on the title page of this CPI document.

* 

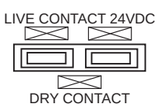
DRY CONTACT POSITION FOR JW1 TO JW5 SHOWN. JUMPER CONNECTS PINS 4-6



LIVE CONTACT POSITION FOR JW1 TO JW5 SHOWN. JUMPER CONNECTS PINS 6-8

** 

DRY CONTACT POSITION FOR JW6 TO JW8 SHOWN. JUMPER CONNECTS PINS 2-3



LIVE CONTACT 24VDC POSITION FOR JW6 TO JW8 SHOWN. JUMPERS CONNECT PINS 1-2 AND 3-4

***

THESE JUMPERS MAY NEED TO BE INSERTED IN SOME APPLICATIONS. REFER TO CHAPTER 3B FOR DETAILS.

DRAWN G. SANWALD	DATE 13 APR 2000	**ROOM INTERFACE**
CHECKED S. BLAKE	14 APR 2000	
DES.\MFG.\AUTH. L. FOSKIN	13 APR 2000	**MD-0763 REV K**
		SHEET 2 OF 3

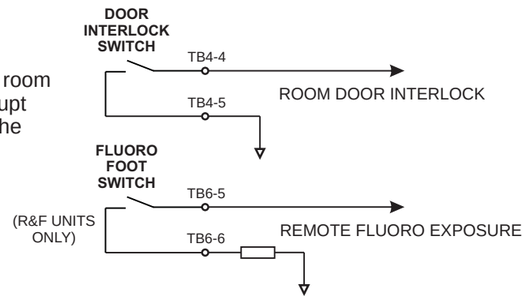
INPUT	DESCRIPTION
SPARE / TABLE STEPPER INPUT	When used with the ***table stepper / kV-mAs reduction for peripheral angiography*** option (used for peripheral runoff studies), this input tells the generator to advance to the next kV/mAs step. When the above option is not enabled, this input may be programmed as a spare input.
BUCKY CONTACTS	This indicates that the Bucky is ready for an exposure (the grid is moving). The outputs of all Buckys must be connected in parallel to this single input.
COLLIMATOR INTERLOCK	This is the input for the collimator interlock. This may be programmed to inhibit exposures if this input is not active.
REMOTE TOMO SELECT	This input, when active, remotely selects tomography.
TOMO EXPOSURE	Requests a tomographic exposure when this input is active. The exposure starts when the input is activated, and stops when the input is deactivated.
ROOM DOOR INTERLOCK	This is the interlock for the X-ray room door. If programmed, will inhibit an exposure when this input is not active.
THERMAL SWITCH 2	Input for the tube 2 thermal switch. Exposures are inhibited when this input is not active. The power supply is also turned off to prevent rotor operation.
THERMAL SWITCH 1	Input for the tube 1 thermal switch. Exposures are inhibited when this input is not active. The power supply is also turned off to prevent rotor operation.
MULTIPLE SPOT EXPOSURE	Enables density compensation when doing multiple exposures on a single film. In this mode of operation, the X-ray field is usually coned down to a small area. Due to the resulting AEC field cutoff, an AEC density offset may be required. This is designated multiple spot compensation. The function **MULT. SPOT COMP** in the AEC calibration menus applies the required compensation.
I.I SAFETY / REMOTE HLF SELECT	Refer to chapter 3B: On applicable units, if the HLF SELECT input is CONSOLE, this will be the input for the image intensifier position interlock. If the HLF SELECT input is REMOTE, this will be the high-level fluoro select input.
REMOTE FLUORO EXPOSURE	Fluoro foot switch input. Fluoro exposures are requested when this input is active.
REMOTE PREP	External PREP request, typically generated by room equipment.
REMOTE EXPOSURE	External X-ray EXPOSE command from room equipment (i.e. table or digital imaging system).

Certain inputs will only be active if enabled in programming (per chapter 3C), and / or the generator includes the corresponding option.

ROOM DOOR INTERLOCKS

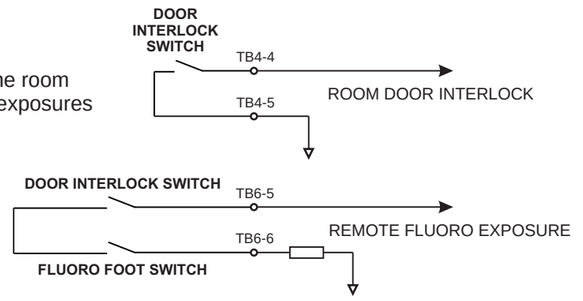
Configuration A

Inhibits new exposures if the room door is open. Does not interrupt exposures in process when the door is opened.



Configuration B

Inhibits new exposures if the room door is open. Stops fluoro exposures if the room door is opened during a fluoro exposure.



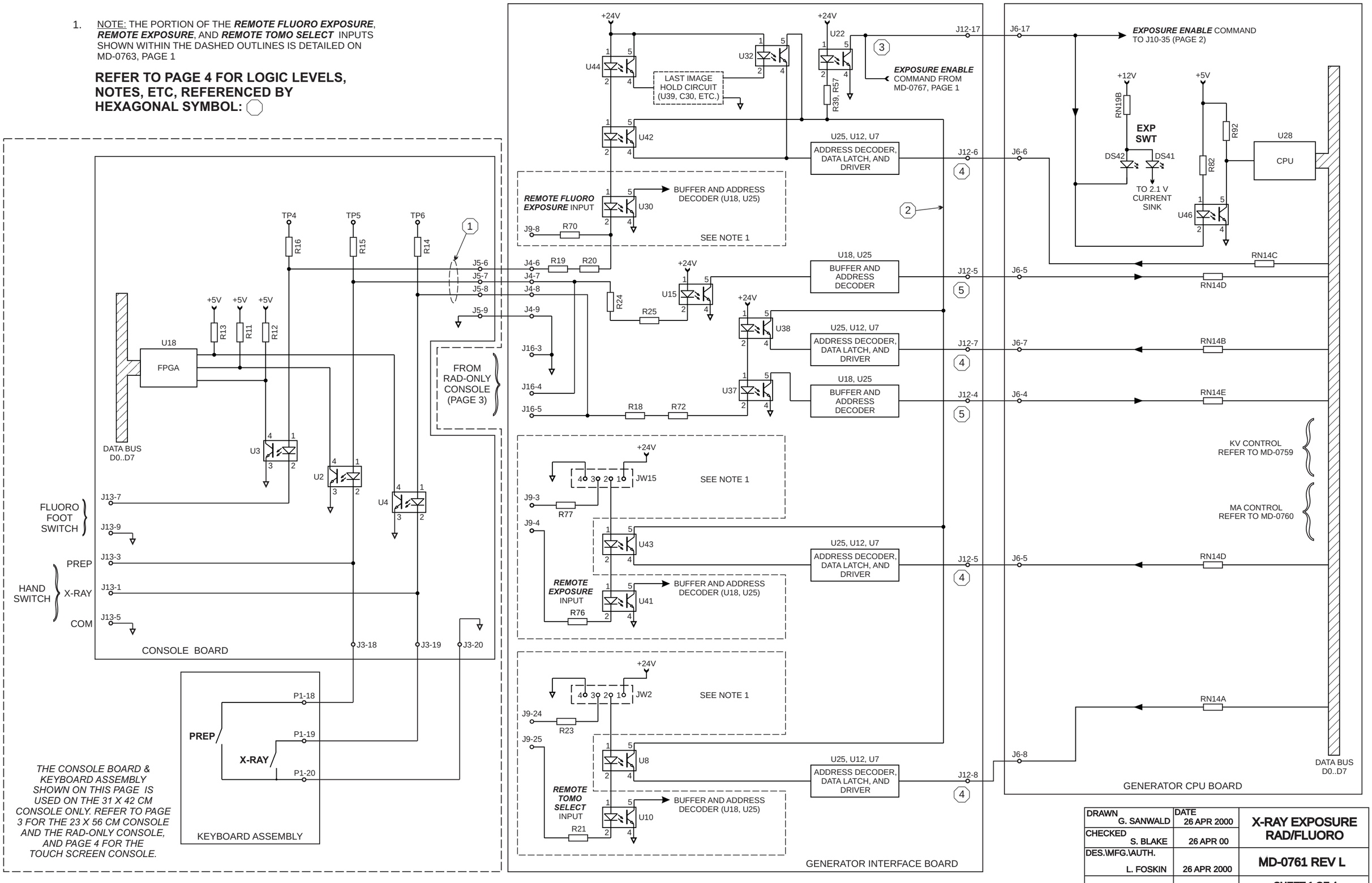
NOTE: For this configuration, the room door interlock switch must be a double-pole type (one pole for the room door interlock, with the second pole in series with the fluoro foot switch).

DRAWN G. SANWALD	DATE 13 APR 2000	ROOM INTERFACE
CHECKED S. BLAKE	14 APR 2000	
DES.\MFG.\AUTH. L. FOSKIN	13 APR 2000	MD-0763 REV K
		SHEET 3 OF 3

Use and disclosure is subject to the restrictions on the title page of this CPI document.

1. NOTE: THE PORTION OF THE ***REMOTE FLUORO EXPOSURE***, ***REMOTE EXPOSURE***, AND ***REMOTE TOMO SELECT*** INPUTS SHOWN WITHIN THE DASHED OUTLINES IS DETAILED ON MD-0763, PAGE 1

REFER TO PAGE 4 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY HEXAGONAL SYMBOL: ⬡



DRAWN G. SANWALD	DATE 26 APR 2000	**X-RAY EXPOSURE RAD/FLUORO**
CHECKED S. BLAKE	26 APR 00	
DES.\MFG.\AUTH. L. FOSKIN	26 APR 2000	**MD-0761 REV L**
		SHEET 1 OF 4

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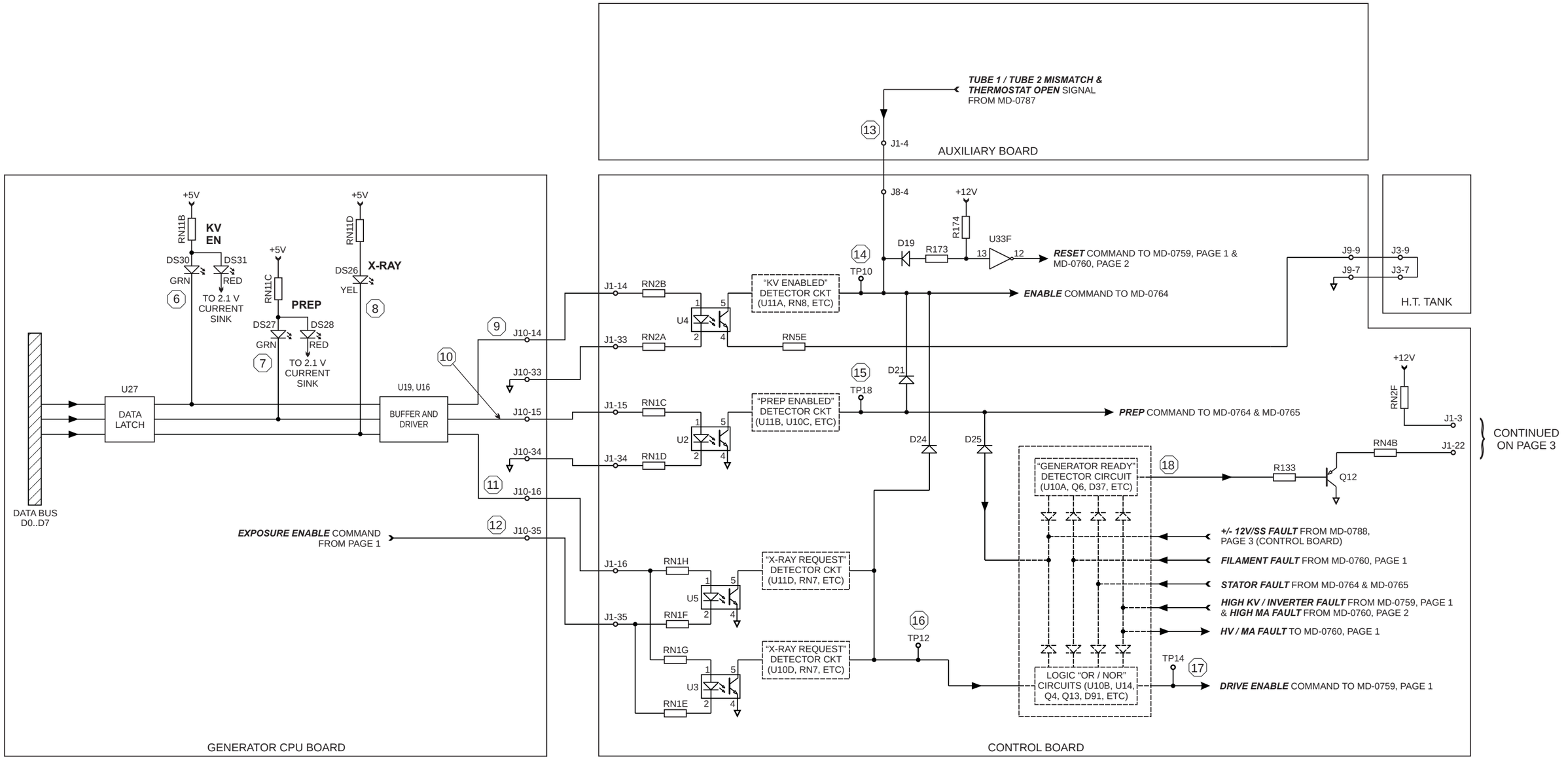
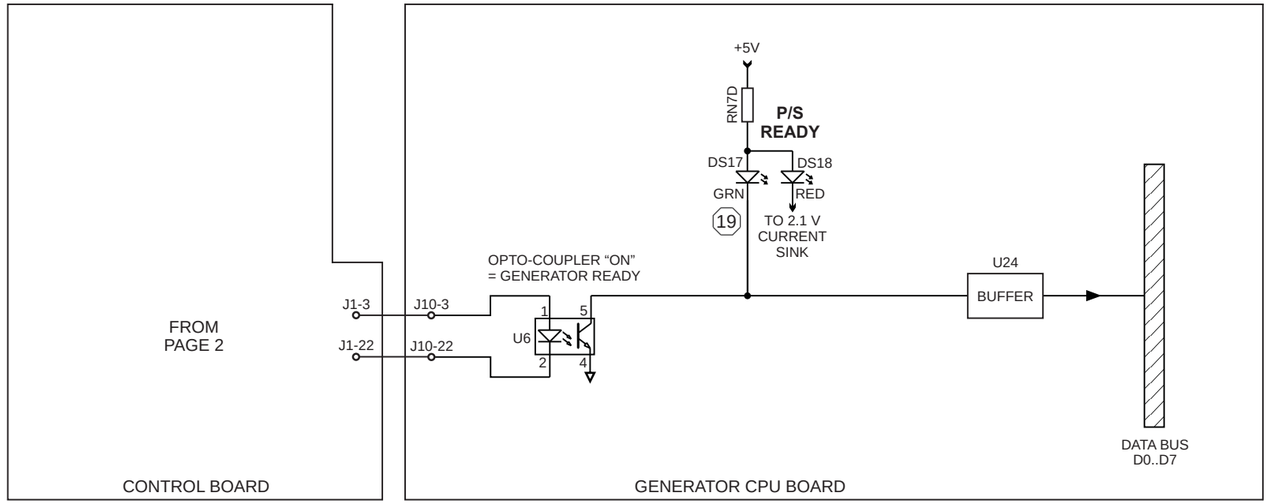
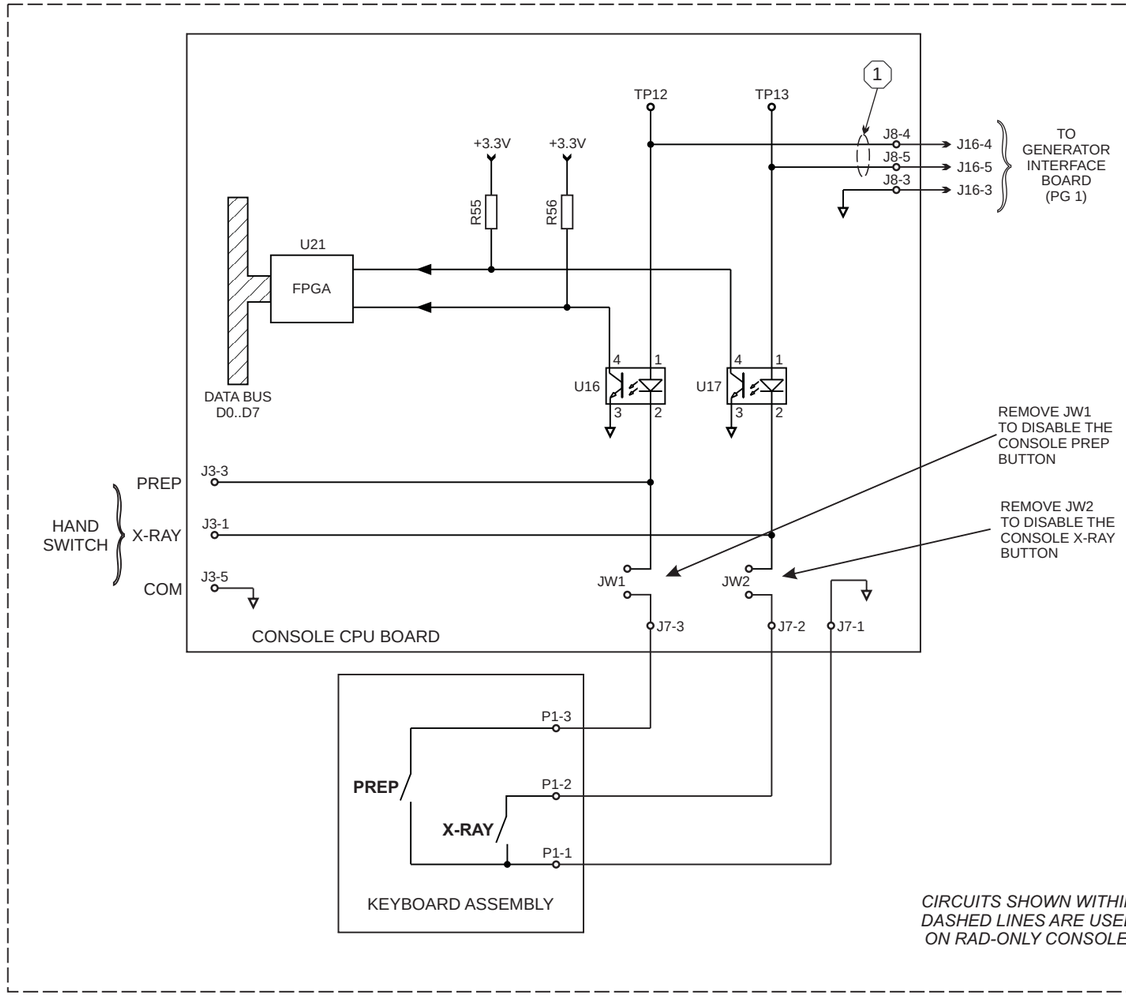
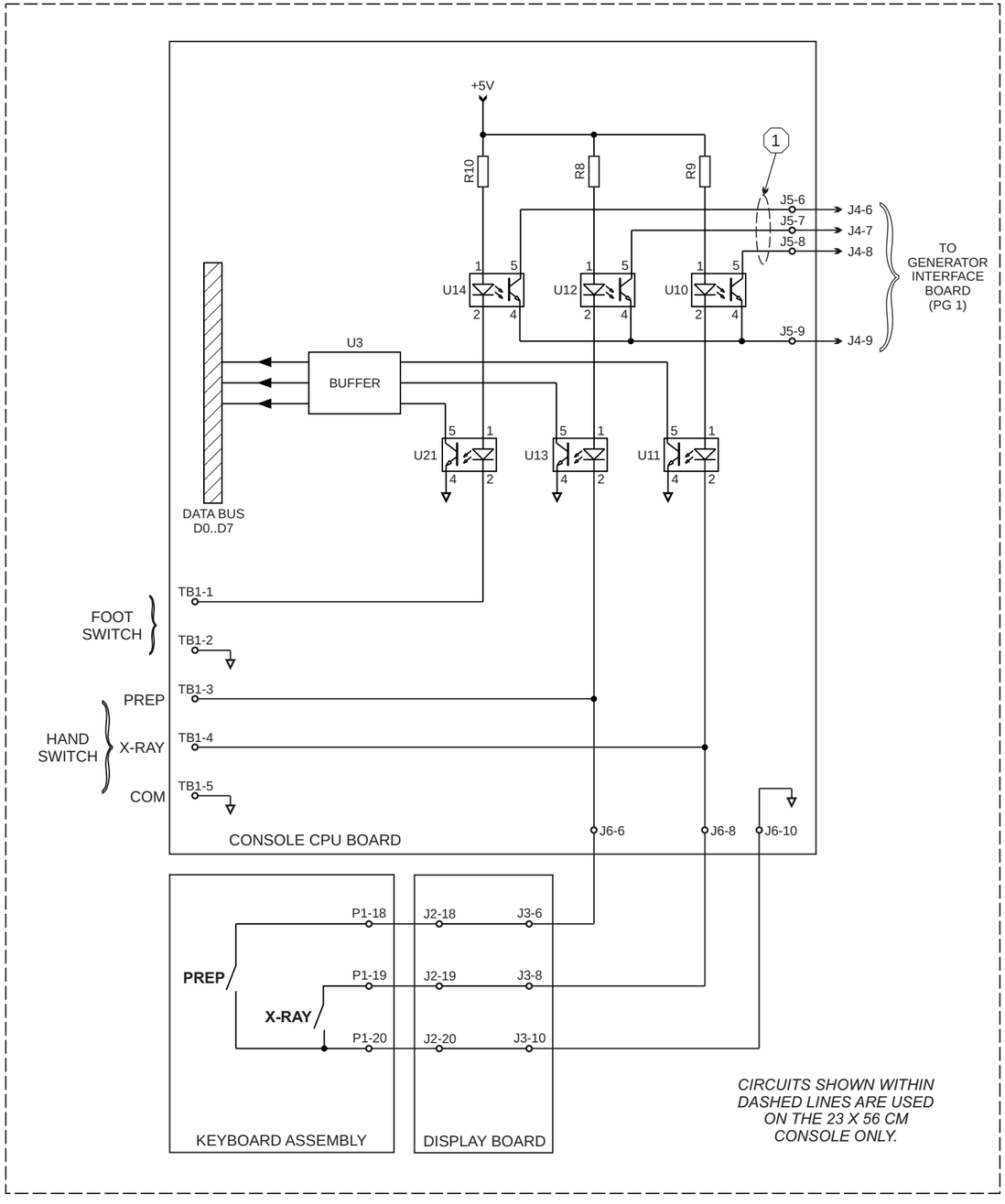


DRAWN G. SANWALD	DATE 26 APR 2000	X-RAY EXPOSURE RAD/FLUORO
CHECKED S. BLAKE	26 APR 00	
DES.\MFG.\AUTH. L. FOSKIN	26 APR 2000	MD-0761 REV L
		SHEET 2 OF 4

Use and disclosure is subject to the restrictions on the title page of this CPI document.







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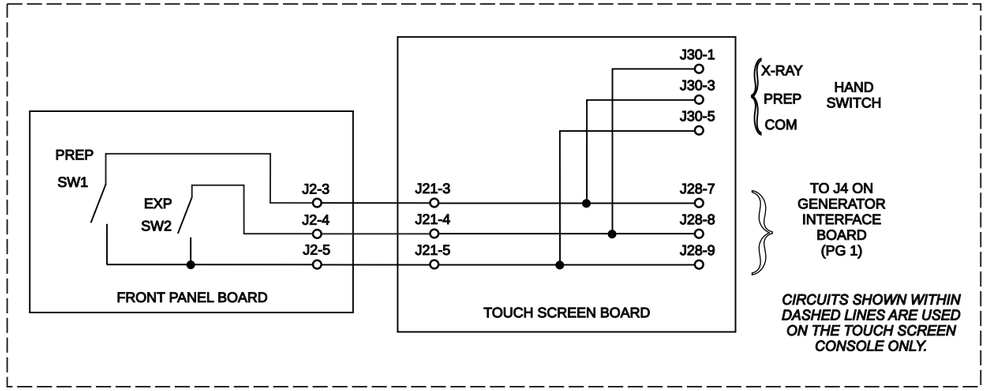
DRAWN G. SANWALD	DATE 26 APR 2000	X-RAY EXPOSURE RAD/FLUORO
CHECKED S. BLAKE	26 APR 00	
DES.\MFG.\AUTH. L. FOSKIN	26 APR 2000	MD-0761 REV L
		SHEET 3 OF 4



NOTE REFERENCE	REMARKS
1	"LOW" (APPROXIMATELY 1 VDC) AT THESE POINTS INDICATES **FOOT SWITCH** INPUT CLOSED, **PREP** SWITCH PRESSED, OR **X-RAY** SWITCH PRESSED RESPECTIVELY. "HIGH" (APPROXIMATELY 24 VDC) = OPEN CIRCUIT (I.E. NOT PRESSED) **FOOT SWITCH**, OR **PREP** SWITCH, OR **X-RAY** SWITCH. FOR RAD-ONLY CONSOLE, "LOW" INDICATES **PREP** SWITCH PRESSED, OR **X-RAY** SWITCH PRESSED, RESPECTIVELY.
2	"LOW" (APPROXIMATELY 1 VDC) = AN X-RAY EXPOSURE HAS BEEN REQUESTED VIA ONE OF SEVERAL EXPOSURE INPUTS. "HIGH" (APPROXIMATELY 24 VDC) = NO X-RAY EXPOSURE HAS BEEN REQUESTED.
3	***EXPOSURE ENABLE*** LINE. "LOW" (APPROXIMATELY 0 VDC) INDICATES AN X-RAY EXPOSURE REQUEST, "HIGH" (APPROXIMATELY 5 VDC) = NO X-RAY EXPOSURE HAS BEEN REQUESTED.
4	THE CATHODE OF THE ASSOCIATED LED IS HELD "LOW" UNDER CPU CONTROL DURING AN X-RAY EXPOSURE REQUEST ONLY. NO MEANINGFUL MEASUREMENTS CAN BE MADE ON THIS LINE AS THIS IS A DATA LINE. THE REQUIRED DATA IS LATCHED BY THE REGISTER CIRCUIT(S) AT THE APPROPRIATE TIME.
5	THE OUTPUT OF THE ASSOCIATED LED IS LATCHED BY A REGISTER. THIS IS THEN READ BY THE DATA BUS AT THE APPROPRIATE TIME. AS THIS IS A DATA LINE, NO MEANINGFUL MEASUREMENTS CAN BE MADE AT THIS CONNECTION.
6	DS30 LIT = KV ENABLE REQUEST SENT. THIS IS NECESSARY TO MAKE AN X-RAY EXPOSURE. DS31 LIT = KV ENABLE NOT REQUESTED.
7	DS27 LIT = **PREP** REQUEST SENT. DS28 LIT = **PREP** NOT REQUESTED.
8	DS26 LIT = X-RAY EXPOSURE IN PROCESS.
9	"HIGH" (APPROXIMATELY 5 VDC) = KV ENABLED, "LOW" (APPROXIMATELY 0 VDC) = KV NOT ENABLED.
10	"HIGH" (APPROXIMATELY 5 VDC) = **PREP** REQUESTED. "LOW" (APPROXIMATELY 0 VDC) = **PREP** NOT REQUESTED.
11	"HIGH" (APPROXIMATELY 5 VDC) = **X-RAY** REQUESTED. "LOW" (APPROXIMATELY 0 VDC) = **X-RAY** NOT REQUESTED.
12	"LOW" = X-RAY EXPOSURE REQUESTED AS PER # 3. THIS LINE MUST BE "LOW" IN ORDER FOR THE X-RAY EXPOSURE LED'S ON THE CONTROL BOARD TO BE ENERGIZED (SEE # 16).
13	"LOW" = (APPROXIMATELY 0 VDC) = ***TUBE 1 / TUBE 2 MISMATCH*** OR ***THERMOSTAT OPEN*** FAULT. "HIGH" (APPROXIMATELY 12 VDC) = NO FAULT.
14	"HIGH" (APPROXIMATELY 12 VDC) = KV ENABLED, "LOW" (APPROXIMATELY 0 VDC) = KV NOT ENABLED.
15	"HIGH" (APPROXIMATELY 12 VDC) = **PREP** REQUESTED, "LOW" (APPROXIMATELY 0 VDC) = **PREP** NOT REQUESTED.
16	"HIGH" (APPROXIMATELY 12 VDC) = **X-RAY** REQUESTED, "LOW" (APPROXIMATELY 0 VDC) = **X-RAY** NOT REQUESTED.
17	"HIGH" (APPROXIMATELY 5 VDC) = OUTPUT DRIVE ENABLED, "LOW" (APPROXIMATELY 0 VDC) = OUTPUT DRIVE DISABLED.
18	ALL INPUTS TO THE "GENERATOR READY DETECTOR CIRCUIT" MUST BE AT THE CORRECT LOGIC LEVEL IN ORDER TO BE ABLE TO MAKE AN X-RAY EXPOSURE. THIS MEANS ALL FOUR FAULT INPUTS SHOWN MUST BE CLEARED, AND THE **KV ENABLE** AND **PREP** COMMANDS MUST BE PRESENT.
19	DS17 LIT INDICATES GENERATOR READY TO MAKE AN EXPOSURE. THIS REQUIRES THAT ALL CONDITIONS PER # 18 BE SATISFIED. DS18 LIT INDICATES A "GENERATOR READY DETECTOR CIRCUIT" INPUT IS NOT SATISFIED TO ENABLE AN X-RAY EXPOSURE.

DRAWN G. SANWALD	DATE 26 APR 2000	**X-RAY EXPOSURE RAD/FLUORO**
CHECKED S. BLAKE	26 APR 00	
DES.\MFG.\AUTH. L. FOSKIN	26 APR 2000	**MD-0761 REV L**
		SHEET 4 OF 4

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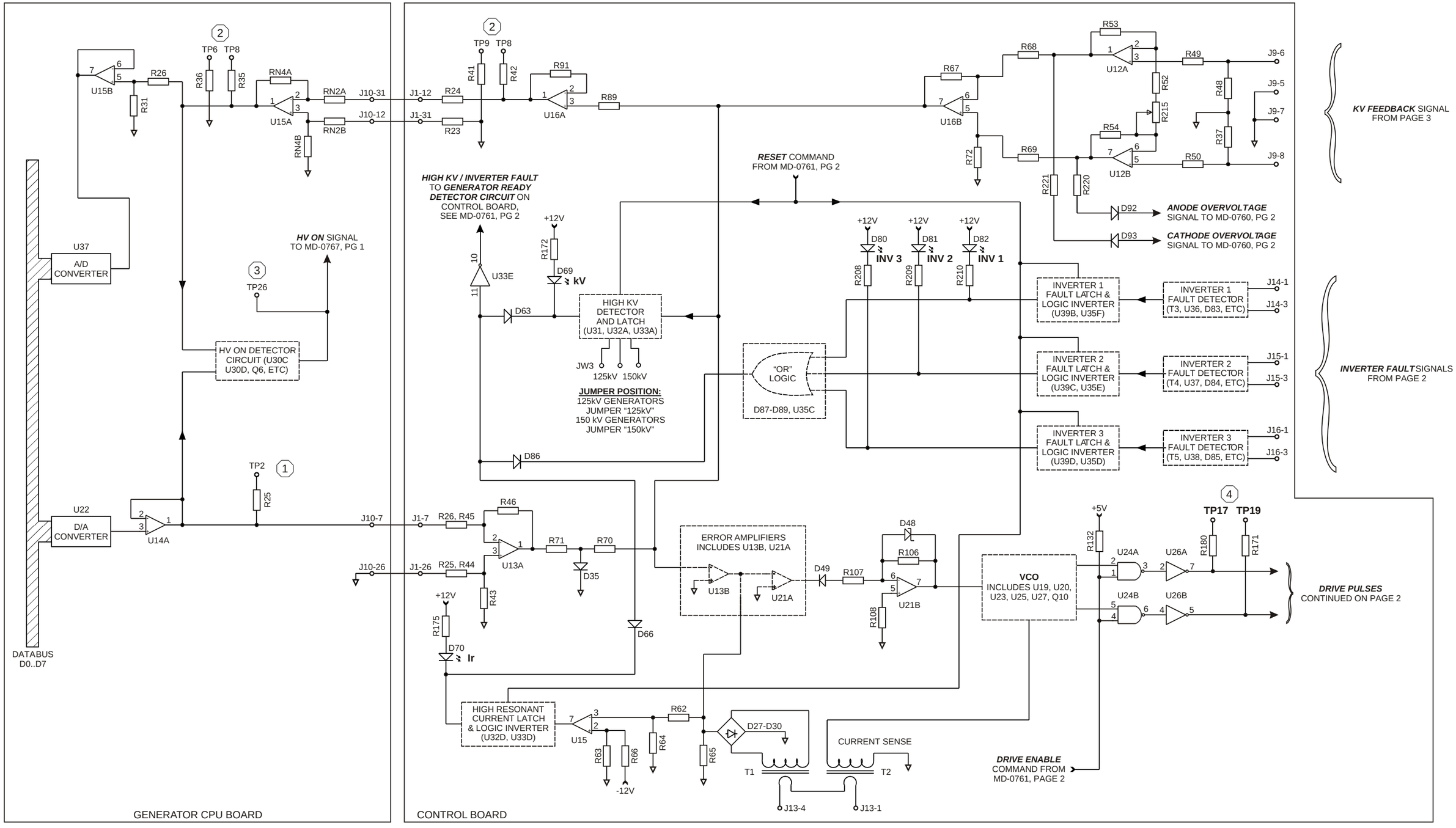

DRAWN G. SANWALD	DATE 18 MAY 2000	KV CONTROL & FEEDBACK
CHECKED S. BLAKE	18 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	18 MAY 2000	MD-0759 REV E
		SHEET 1 OF 4

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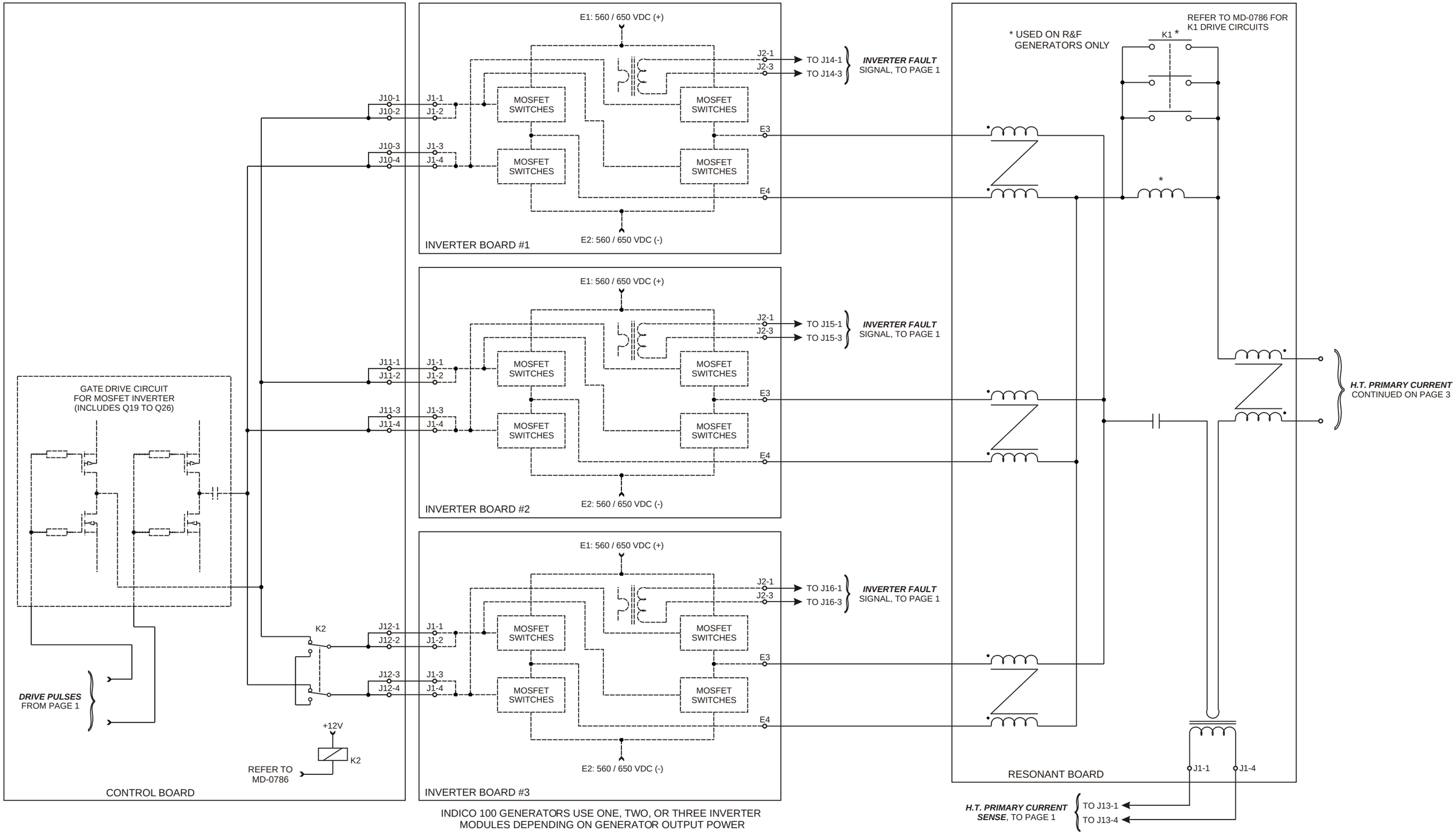
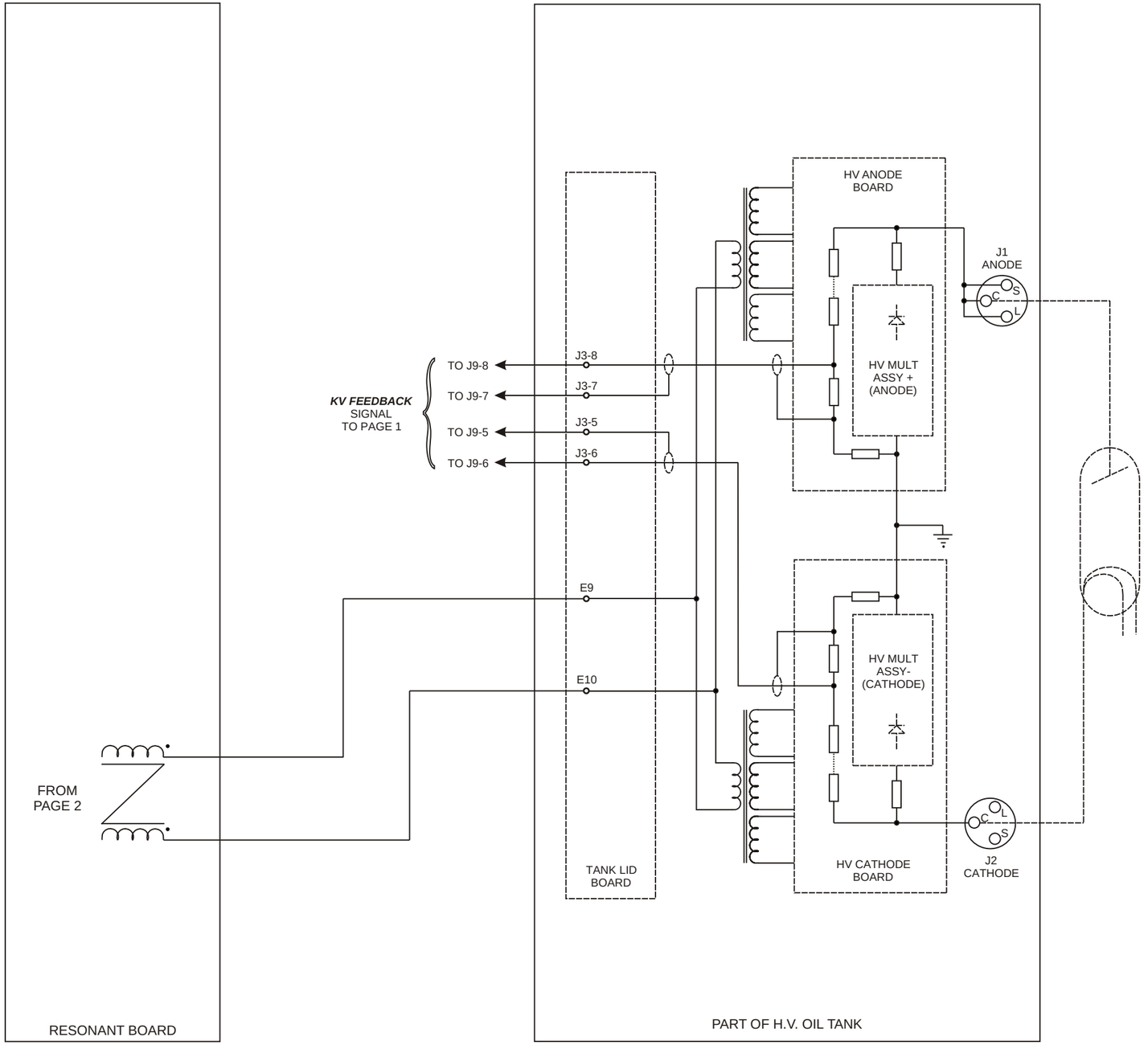


INDICO 100 GENERATORS USE ONE, TWO, OR THREE INVERTER MODULES DEPENDING ON GENERATOR OUTPUT POWER

DRAWN G. SANWALD	DATE 18 MAY 2000	KV CONTROL & FEEDBACK
CHECKED S. BLAKE	18 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	18 MAY 2000	MD-0759 REV E
		SHEET 2 OF 4

Use and disclosure is subject to the restrictions on the title page of this CPI document.



** ONE TUBE H.T. OUTPUTS ARE SHOWN. TWO TUBE TANKS WILL HAVE A SECOND PAIR OF H.T. OUTPUTS

DRAWN G. SANWALD	DATE 18 MAY 2000	KV CONTROL & FEEDBACK
CHECKED S. BLAKE	18 MAY 2000	
DES.\MFG.\AUTH. L.FOSKIN	18 MAY 2000	MD-0759 REV E
		SHEET 3 OF 4

Use and disclosure is subject to the restrictions on the title page of this CPI document.

NOTE REFERENCE	REMARKS
1	kV REFERENCE OUTPUT, GENERATED BY THE CPU. SCALING IS 1 VOLT OUT = 15 kV OF GENERATOR OUTPUT.
2	kV FEEDBACK TO THE CPU. SCALING IS 1V = 20 KV OF GENERATOR OUTPUT.
3	***HV ON*** SIGNAL. THIS IS “HIGH” (APPROXIMATELY 5 VDC) WHEN HIGH VOLTAGE IS ON, “LOW” (APPROXIMATELY 0 VDC) WHEN HIGH VOLTAGE IS OFF.
4	THE VOLTAGE AT TP17 AND TP19 SHOULD BE A 50% DUTY CYCLE SQUARE WAVE, RANGING IN FREQUENCY FROM APPROXIMATELY 80 kHz TO APPROXIMATELY 250 kHz, DEPENDING ON GENERATOR OUTPUT POWER. SEE FIGURE 1.

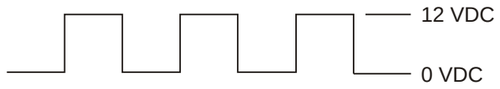
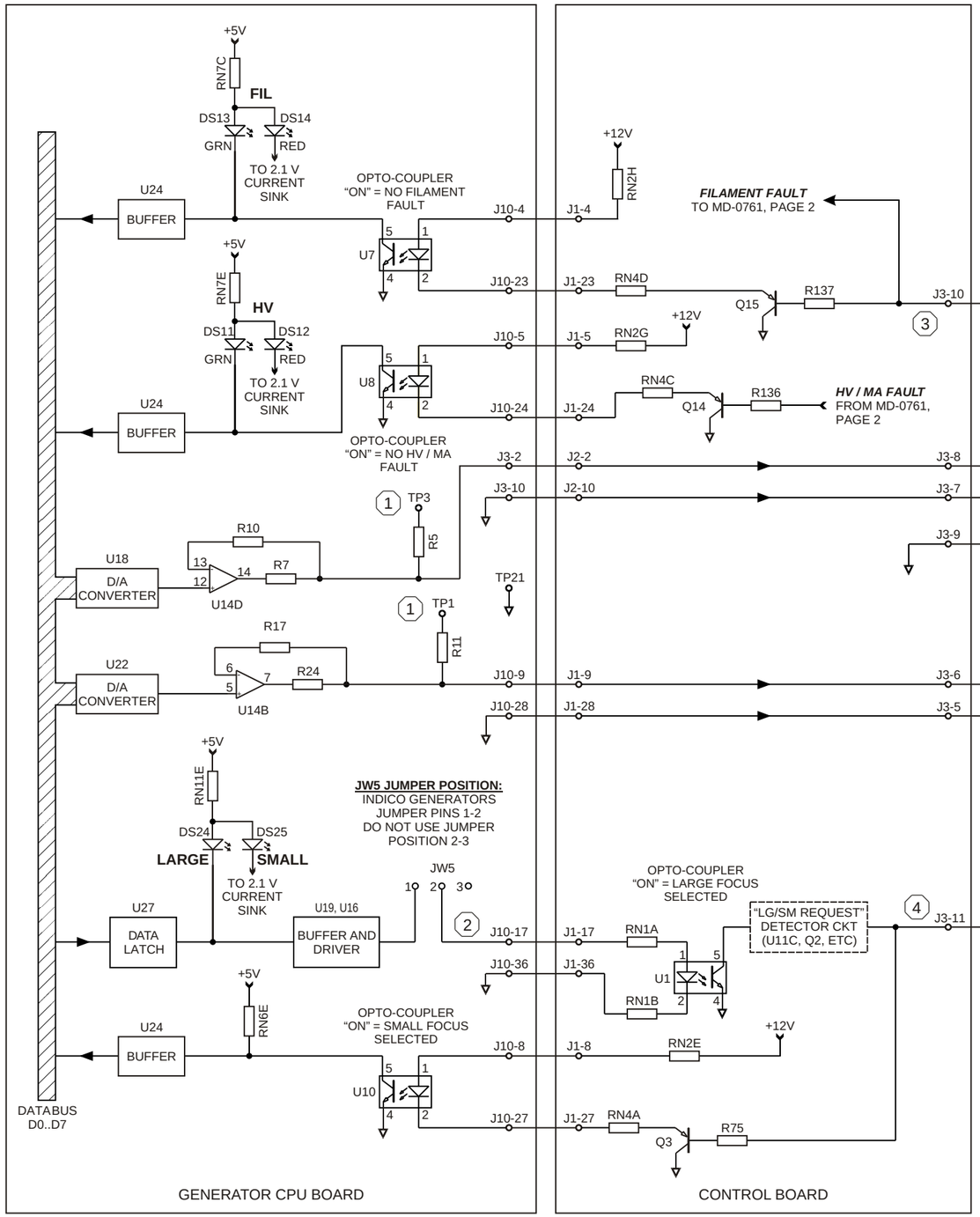
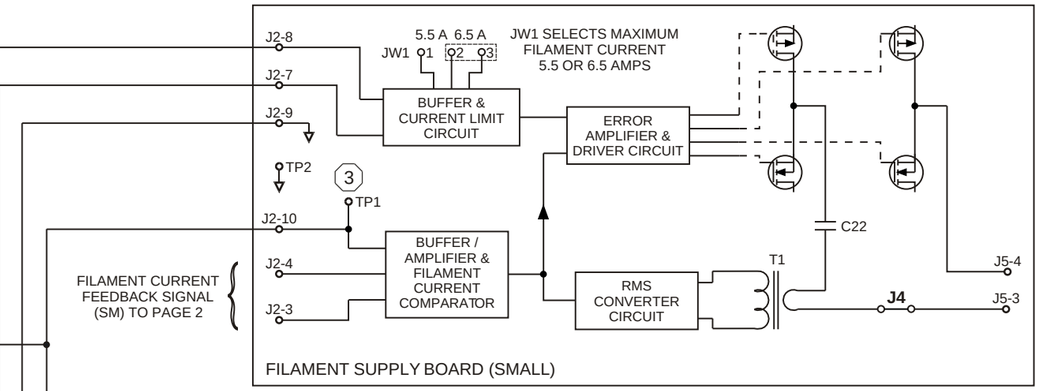


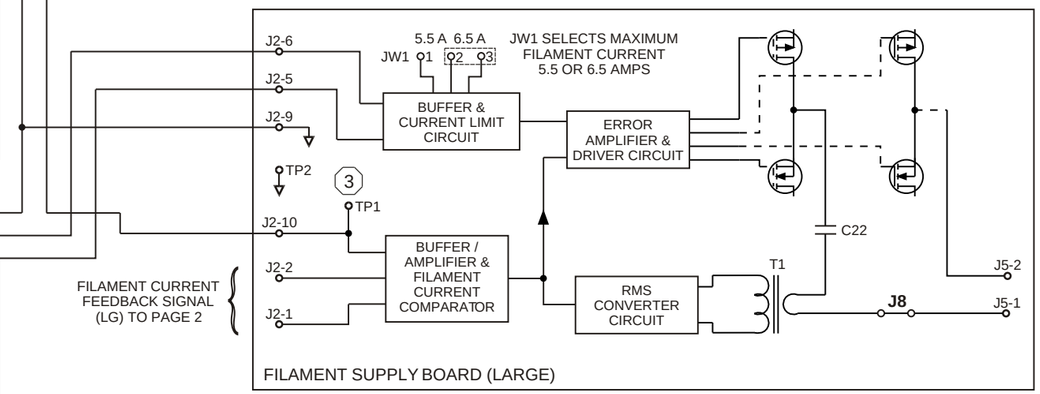
FIGURE 1

DRAWN G. SANWALD	DATE 18 MAY 2000	KV CONTROL & FEEDBACK
CHECKED S. BLAKE	18 MAY 2000	
DES.\MFG.\AUTH. L.FOSKIN	18 MAY 2000	MD-0759 REV E
		SHEET 4 OF 4

Use and disclosure is subject to the restrictions on the title page of this CPI document.

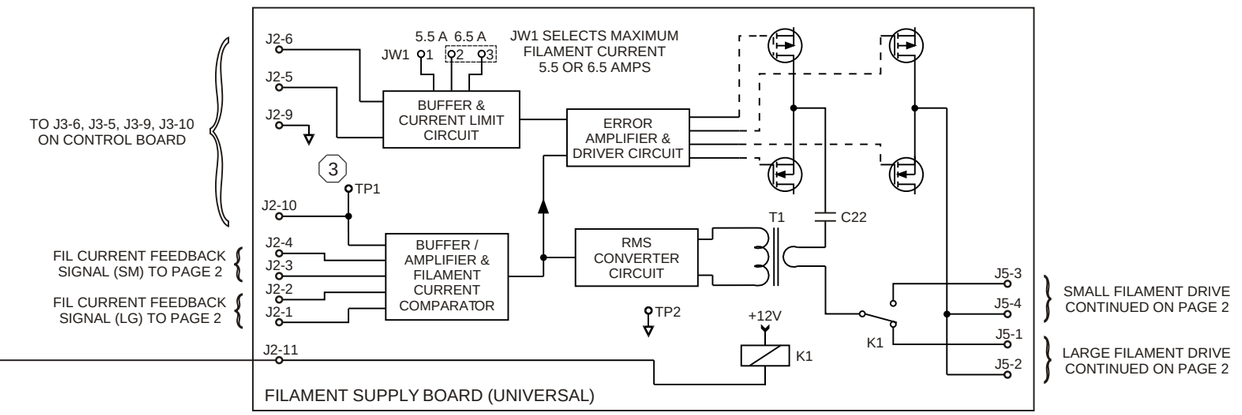






INDICO 100 GENERATORS WITH OPTIONAL TWO FILAMENT BOARDS (TYPICALLY USED IN R&F GENERATORS) USE THE FILAMENT BOARD CONFIGURATION SHOWN ABOVE

INDICO 100 GENERATORS WITH STANDARD SINGLE FILAMENT BOARD (TYPICALLY USED IN RAD ONLY GENERATORS) USE THE FILAMENT BOARD CONFIGURATION SHOWN BELOW

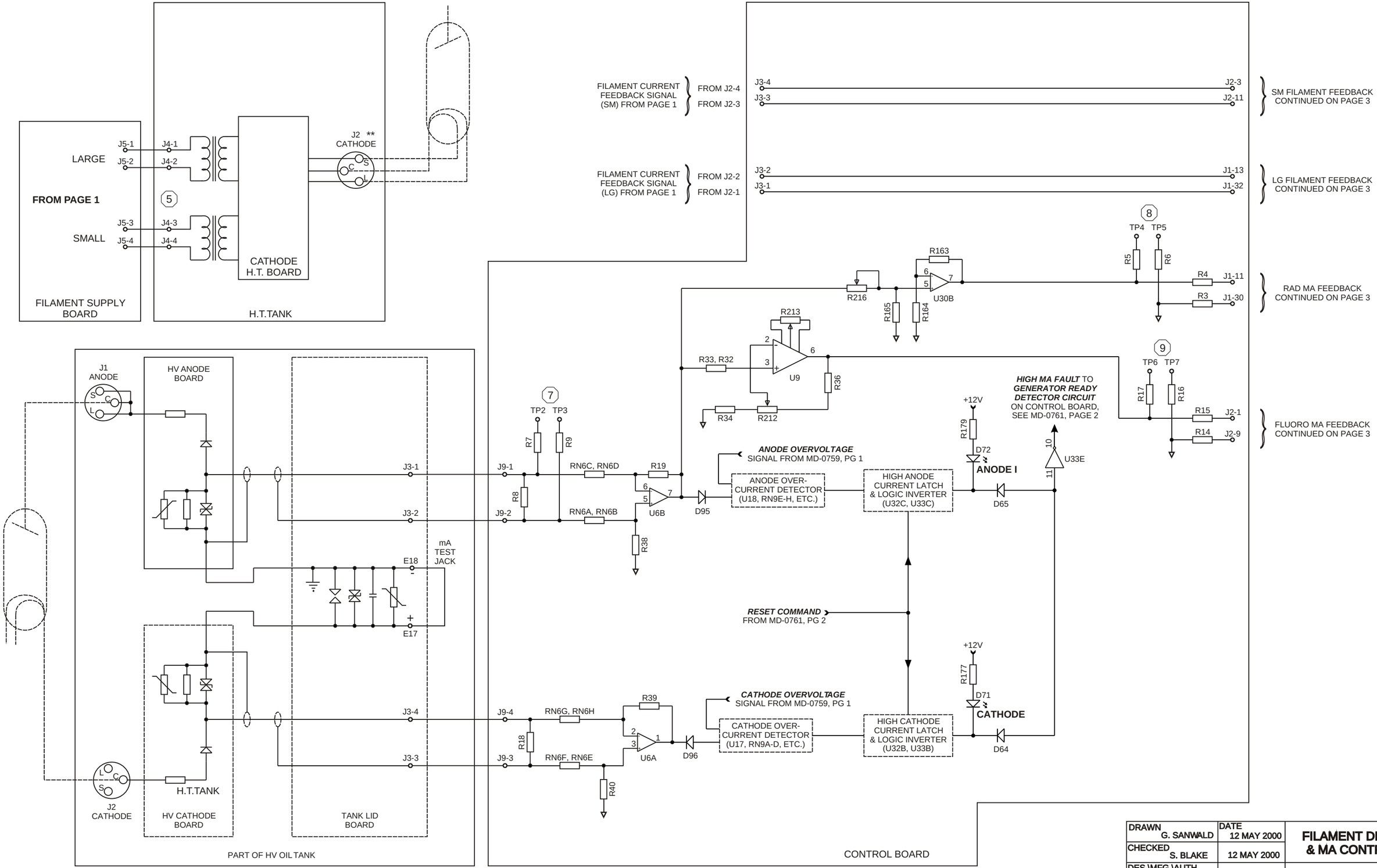


REFER TO PAGE 4 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY HEXAGONAL SYMBOL: ⬡

DUE TO SPACE RESTRICTIONS, THIS PAGE SHOWS ONLY THE MAJOR FILAMENT BLOCKS. REFER TO PAGE 3 FOR A MORE DETAILED FUNCTIONAL DIAGRAM OF THE FILAMENT SUPPLY BOARD.

DRAWN G. SANWALD	DATE 12 MAY 2000	**FILAMENT DRIVE & MA CONTROL**
CHECKED S. BLAKE	12 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	15 MAY 2000	**MD-0760 REV G**
		SHEET 1 OF 4

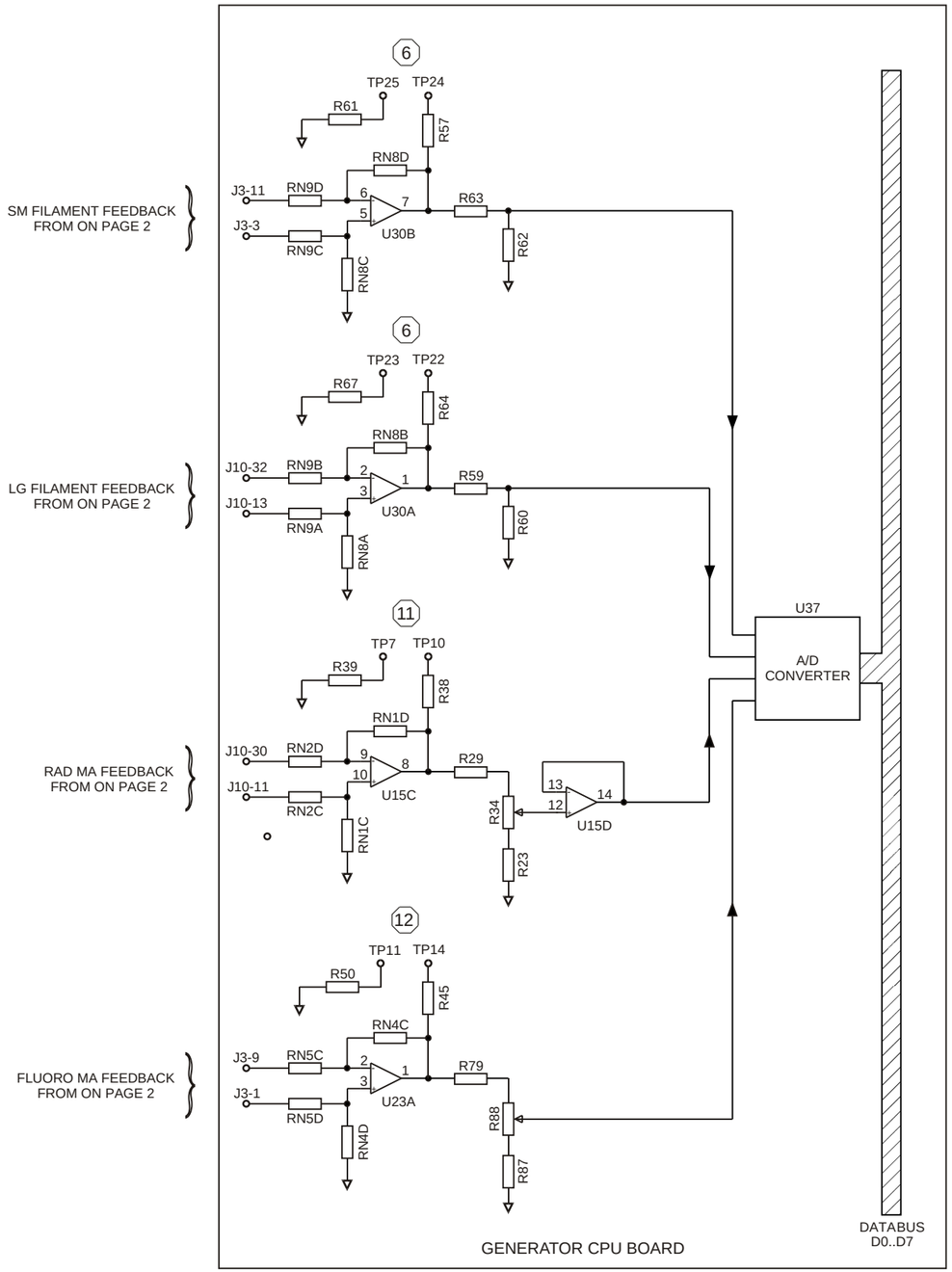
Use and disclosure is subject to the restrictions on the title page of this CPI document.

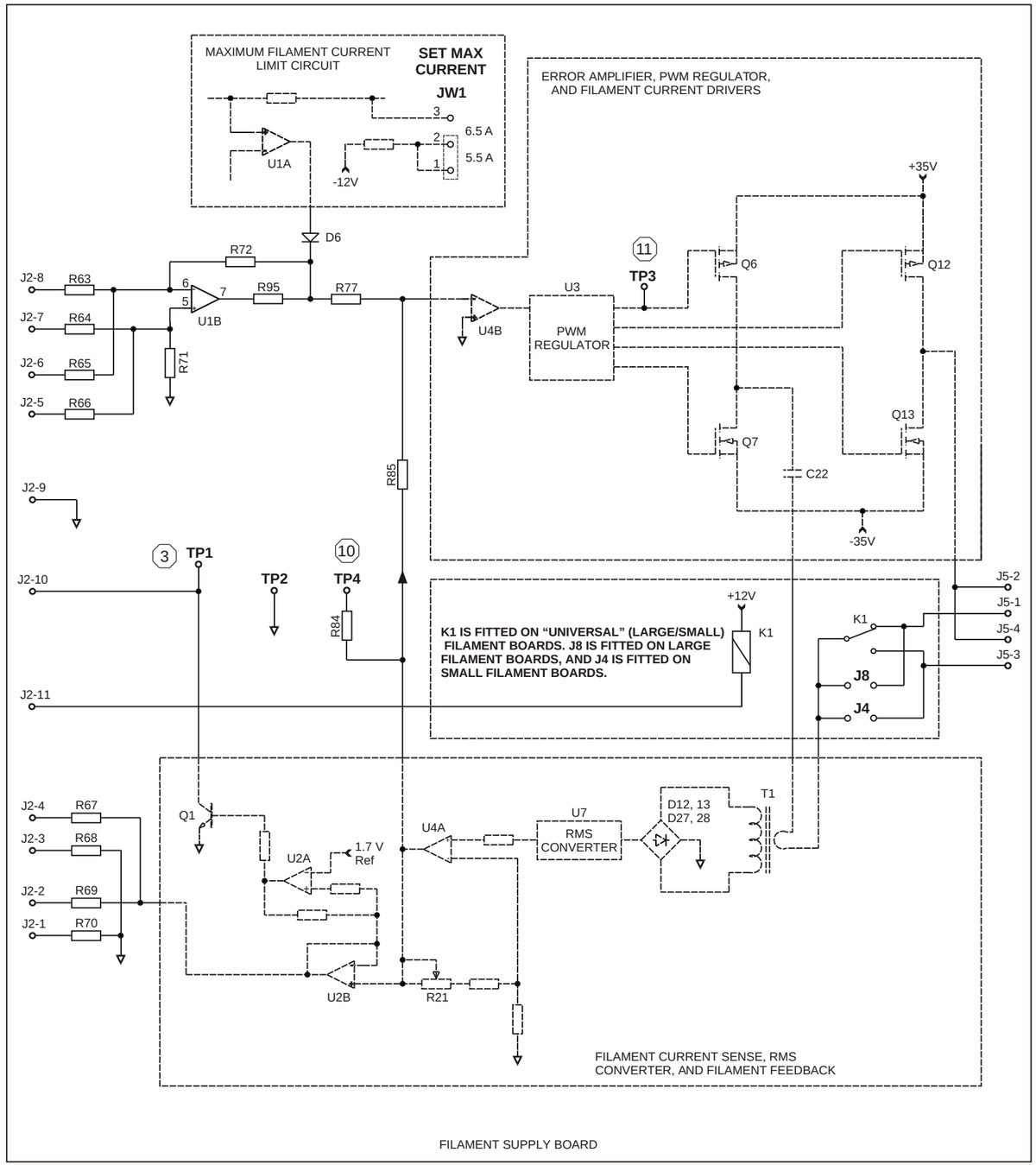


** ONE TUBE H.T. OUTPUTS ARE SHOWN. TWO TUBE TANKS WILL HAVE A SECOND PAIR OF H.T. OUTPUTS

DRAWN G. SANWALD	DATE 12 MAY 2000	**FILAMENT DRIVE & MA CONTROL**
CHECKED S. BLAKE	12 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	15 MAY 2000	**MD-0760 REV G**
		SHEET 2 OF 4

Use and disclosure is subject to the restrictions on the title page of this CPI document.





DRAWN G. SANWALD	DATE 12 MAY 2000	**FILAMENT DRIVE & MA CONTROL**
CHECKED S. BLAKE	12 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	15 MAY 2000	**MD-0760 REV G**
		SHEET 3 OF 4

Use and disclosure is subject to the restrictions on the title page of this CPI document.

NOTE REFERENCE	REMARKS
1	FILAMENT REFERENCE OUTPUTS, GENERATED BY THE CPU. SCALING IS 1 VOLT OUT = 1 AMP OF FILAMENT CURRENT.
2	“HIGH” (APPROXIMATELY 5 VDC) = LARGE FOCUS SELECTED, “LOW” (APPROXIMATELY 0 VDC) = SMALL FOCUS SELECTED. THIS SIGNAL IS USED IN SINGLE FILAMENT SUPPLY GENERATORS ONLY.
3	“HIGH” (APPROXIMATELY 12 VDC) = FILAMENT FAULT (FILAMENT CURRENT < 2 A). “LOW” (APPROXIMATELY 0 VDC) = NO FILAMENT FAULT.
4	“HIGH” (APPROXIMATELY 12 VDC) = LARGE FOCUS SELECTED, “LOW” (APPROXIMATELY 0 VDC) SMALL FOCUS SELECTED.
5	PRIMARY FILAMENT CURRENT AT THESE POINTS MAY BE CONFIRMED USING A CURRENT PROBE ON ONE OF THE OUTPUT LEADS ON THE **SMALL** OR **LARGE** PAIR OF OUTPUTS.
6	THE VOLTAGE AT THESE TEST POINTS WILL BE APPROXIMATELY 1 VDC = 1 AMP OF FILAMENT CURRENT.
7	THESE TEST POINTS ALLOW MEASUREMENT OF A VOLTAGE PROPORTIONAL TO ANODE CURRENT. THE SCALING IS 0.4 VDC = 100 mA. SHORT EXPOSURE TIMES MUST BE CONSIDERED AND APPROPRIATE MEASUREMENT TECHNIQUES MUST BE USED.
8	THESE TEST POINTS ARE SCALED 1 VDC = 100 mA OF X-RAY CURRENT.
9	THESE TEST POINTS ARE SCALED 1 VDC = 2.5 mA OF X-RAY CURRENT (R&F GENERATORS ONLY).
10	FILAMENT FEEDBACK CURRENT TEST POINT. THIS IS SCALED 1 VDC = 1 AMP OF FILAMENT CURRENT.
11	PWM OUTPUT. THE WAVEFORM WILL BE AS PER FIGURE 1 FOR LOW AND HIGH FILAMENT CURRENT DEMAND.

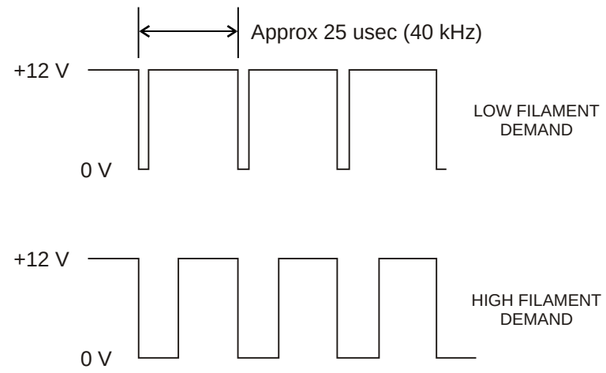
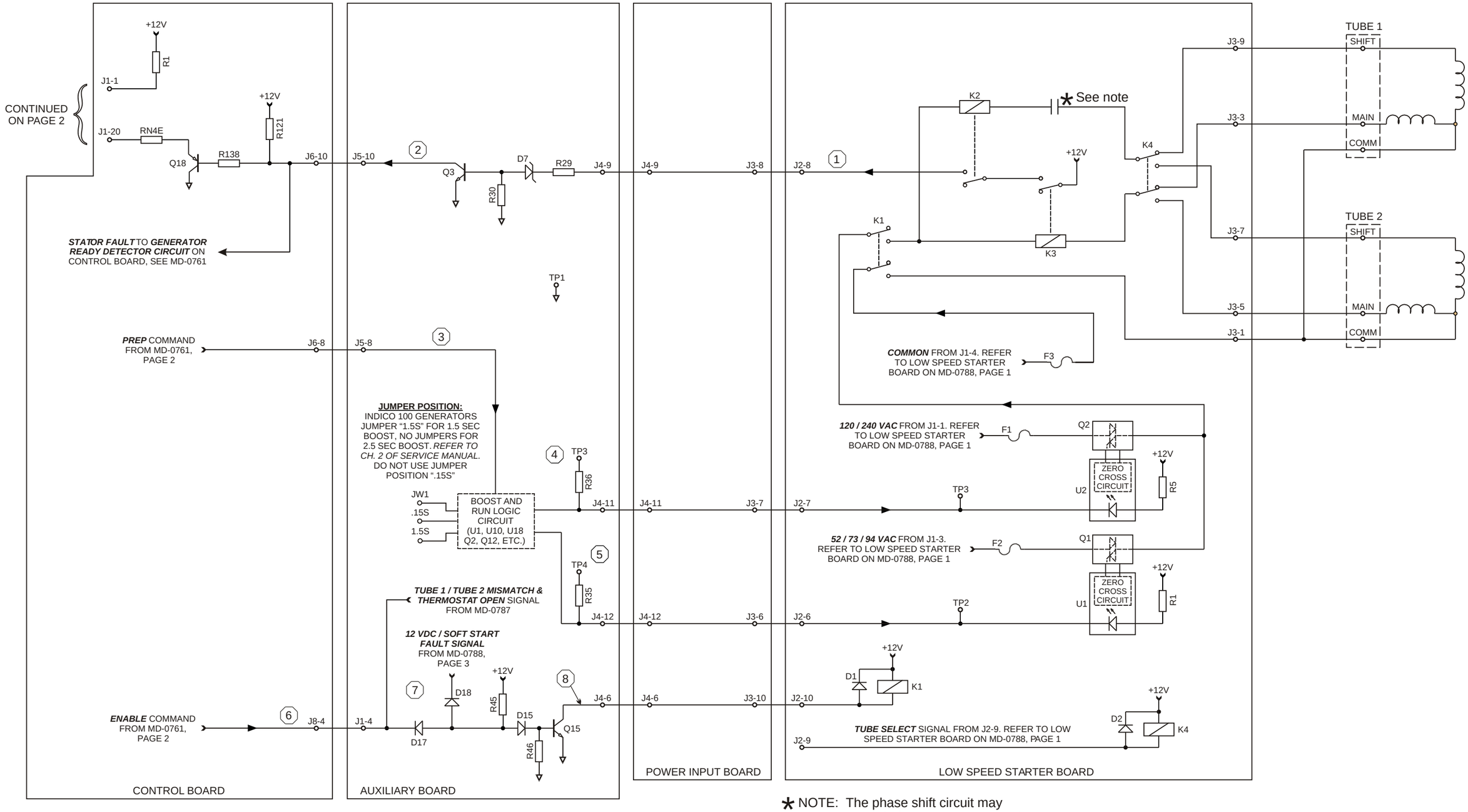


FIGURE 1

DRAWN G. SANWALD	DATE 12 MAY 2000	FILAMENT DRIVE & MA CONTROL
CHECKED S. BLAKE	12 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	15 MAY 2000	MD-0760 REV G
		SHEET 4 OF 4

Use and disclosure is subject to the restrictions on the title page of this CPI document.

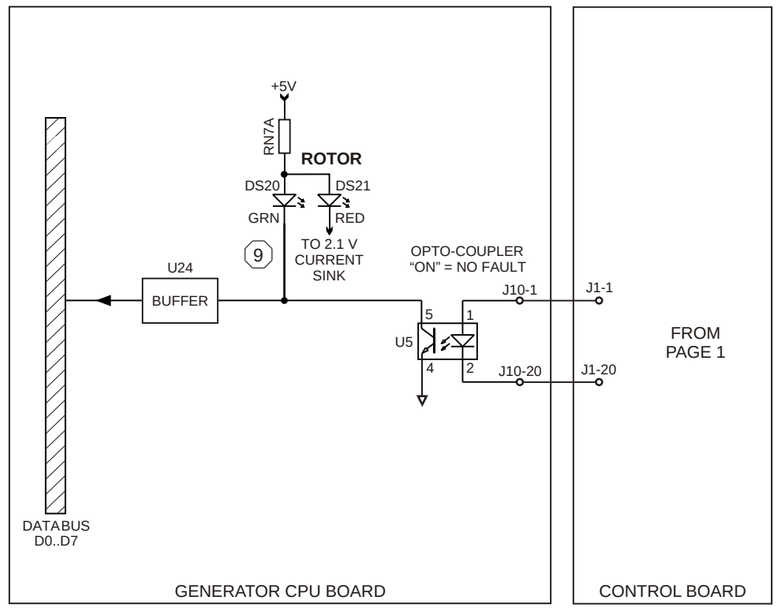
REFER TO PAGE 2 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY HEXAGONAL SYMBOL: ⬡



✱ NOTE: The phase shift circuit may consist of one or more capacitor

DRAWN G. SANWALD	DATE 10 MAR 2000	**LOW SPEED STARTER**
CHECKED _____	_____	
DES.\MFG.\AUTH. HTW	10 MAR 2000	**MD-0764 REV G**
		SHEET 1 OF 2

Use and disclosure is subject to the restrictions on the title page of this CPI document.



NOTE REFERENCE	REMARKS
1	"HIGH" (APPROXIMATELY 6-11 VDC) = NO STATOR FAULT, "LOW" (<APPROXIMATELY 2 VDC) = STATOR FAULT (LOW OR NO STATOR CURRENT).
2	"LOW" (APPROXIMATELY 0 VDC) = NO STATOR FAULT, "HIGH" (APPROXIMATELY 12 VDC) = STATOR FAULT (LOW OR NO STATOR CURRENT).
3	"HIGH" (APPROXIMATELY 10 VDC) = **PREP** REQUESTED, "LOW" (APPROXIMATELY 1 VDC) = **PREP** NOT REQUESTED.
4	"LOW" (APPROXIMATELY 0 VDC) = BOOST REQUESTED, "HIGH" (APPROXIMATELY 12 VDC) = BOOST NOT REQUESTED (BOOST REQUESTED FOR APPROXIMATELY 1.5 SEC AFTER **PREP** INITIATED).
5	"LOW" (APPROXIMATELY 0 VDC) = RUN REQUESTED, "HIGH" (APPROXIMATELY 12 VDC) = RUN NOT REQUESTED (RUN REQUESTED AFTER BOOST COMPLETE, AND FOR DURATION THAT **PREP** IS PRESSED).
6	"HIGH" (APPROXIMATELY 12 VDC) = LOW SPEED STARTER **ENABLED**, "LOW" (APPROXIMATELY 0 VDC) = STARTER DISABLED (SEE # 7).
7	THIS POINT MUST BE "HIGH" (AS PER # 6) TO ENABLE THE LOW SPEED STARTER. THIS REQUIRES THE ***ENABLE*** COMMAND TO BE PRESENT ("HIGH"), AND THE ***TUBE 1 /TUBE 2 MISMATCH &THERMOSTAT OPEN*** SIGNAL TO BE "HIGH". IF THE ***12 VDC / SOFT START FAULT SIGNAL*** IS LOW (INDICATING A FAULT), J1-4 WILL NOT BE PULLED LOW DUE TO THE DIODE SHOWN CONNECTED TO THIS PIN ON PAGE 1.
8	"LOW" (APPROXIMATELY 0 VDC) ENERGIZES K1 ON THE LOW SPEED STARTER BOARD, ENABLING THE STARTER. "HIGH" (APPROXIMATELY 12 VDC) DE-ENERGIZES K1 ON THE LOW SPEED STARTER BOARD. AS PER # 6 AND 7, NO ***ENABLE*** COMMAND, OR PRESENCE OF A ***TUBE 1 / TUBE 2 MISMATCH & THERMOSTAT OPEN FAULT***, OR A ***12 VDC / SOFT START FAULT*** WILL INHIBIT LOW SPEED STARTER OPERATION.
9	DS20 LIT INDICATES NORMAL STATOR CURRENTS. DS 21 LIT INDICATES STATOR FAULT, OR LOW SPEED STARTER IS IN STANDBY MODE.

DRAWN G. SANWALD	DATE 10 MAR 2000	**LOW SPEED STARTER**
CHECKED _____	_____	
DES.\MFG.\AUTH. HTW	10 MAR 2000	**MD-0764 REV G**
		SHEET 2 OF 2

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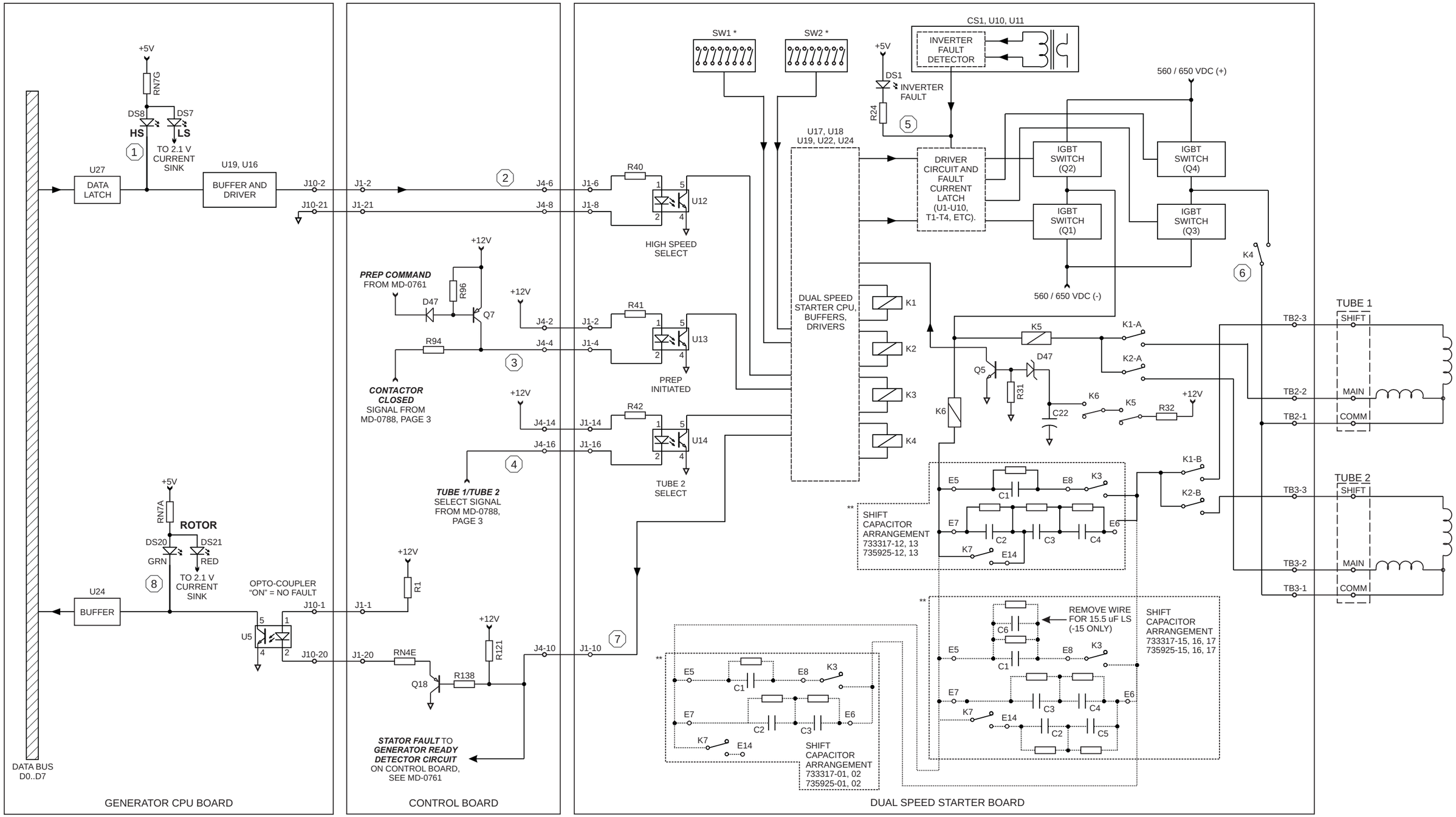

* REFER TO CHAPTER 2 OF SERVICE MANUAL FOR THE PROCEDURE TO SET DIP SWITCHES SW1 AND SW2

** REFER TO SHEET 2 FOR SHIFT CAPACITOR VALUES

DRAWN G. SANWALD	DATE 30 MAR 2000	**DUAL SPEED STARTER**
CHECKED STEVE BLAKE	30 MAR 2000	
DES.\MFG.\AUTH. L.FOSKIN	30 MAR 2000	**MD-0765 REV E**
		SHEET 1 OF 2

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	DUAL SPEED STARTER ASSY								
			733317-01 735925-01	733317-02 735925-02	733317-12 735925-12	733317-13 735925-13	733317-15 735925-15	733317-16 735925-16	733317-17 735925-17
	K3	K7							
LOW SPD (1)	CLOSED	OPEN	31 uF	60 uF	36 uF	30 uF	15.5 / 28 uF	31 uF	30 uF
LOW SPD (2)	CLOSED	CLOSED			37.5 uF	31 uF	N/A	37.5 uF	37.5 uF
HIGH SPD (1)	OPEN	OPEN	6 uF	20 uF	6 uF	5 uF	3 uF	6 uF	5 uF
HIGH SPD (2)	OPEN	CLOSED			7.5 uF	6 uF	6 uF	12.5 uF	12.5 uF

	DUAL SPD STARTER ASSY 733317-01 735925-01	DUAL SPD STARTER ASSY 733317-02 735925-02	DUAL SPD STARTER ASSY 733317-12 735925-12	DUAL SPD STARTER ASSY 733317-13 735925-13	DUAL SPD STARTER ASSY 733317-15 735925-15	DUAL SPD STARTER ASSY 733317-16 735925-16	DUAL SPD STARTER ASSY 733317-17 735925-17
CAPACITOR	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
C1	25 uF	40 uF	30 uF	25 uF	12.5 uF	25 uF	25 uF
C2	N/A	N/A	30 uF	25 uF	6 uF	12.5 uF	15 uF
C3	12.5 uF	40 uF	15 uF	12.5 uF	6 uF	12.5 uF	10 uF
C4	12.5 uF	40 uF	15 uF	12.5 uF	6 uF	12.5 uF	10 uF
C5	N/A	N/A	N/A	N/A	6 uF	12.5 uF	15 uF
C6	N/A	N/A	N/A	N/A	12.5 uF	N/A	N/A

NOTE REFERENCE	REMARKS
1	DS8 LIT INDICATES HIGH SPEED SELECTED, DS7 LIT INDICATES LOW SPEED SELECTED.
2	“HIGH” (APPROXIMATELY 5 VDC) = HIGH SPEED SELECTED, “LOW” (APPROXIMATELY 0 VDC) = LOW SPEED SELECTED.
3	“LOW” (APPROXIMATELY 7 VDC) = CONTACTOR CLOSED **AND** PREP REQUESTED. THIS INITIATES THE BOOST CYCLE. “HIGH” (APPROXIMATELY 12 VDC) = BOOST NOT REQUESTED (PREP COMMAND NOT RECEIVED, OR CONTACTOR IS NOT CLOSED).
4	“LOW” (APPROXIMATELY 0 VDC) = TUBE 2 SELECTED, “HIGH” (APPROXIMATELY 12 VDC) = TUBE 2 DESELECTED. THIS CONDITION DEFAULTS TO TUBE 1.
5	DS1 LIT INDICATES AN INVERTER CURRENT FAULT. POSSIBLE CAUSES INCLUDE INCORRECT DIP SWITCH SETTINGS FOR THE TUBE IN USE (SEE ** ON PAGE 1), INCORRECT STATOR IMPEDANCE, OR DEFECTIVE STATOR CABLE.
6	K4 OPEN CIRCUITS THE STATOR COMMON LEAD AT ALL TIMES THAT THE DUAL SPEED STARTER IS IN STANDBY MODE.
7	“LOW” (APPROXIMATELY 0 VDC) = NO STATOR FAULT, “HIGH” (APPROXIMATELY 12 VDC) = STATOR FAULT (LOW OR NO STATOR CURRENT).
8	DS20 LIT INDICATES NORMAL STATOR CURRENTS. DS21 LIT INDICATES STATOR FAULT, OR DUAL SPEED STARTER IS IN STANDBY MODE.

DRAWN G. SANWALD	DATE 30 MAR 2000	**DUAL SPEED STARTER**
CHECKED STEVE BLAKE	30 MAR 2000	
DES.\MFG.\AUTH. L.FOSKIN	30 MAR 2000	**MD-0765 REV E**
		SHEET 2 OF 2

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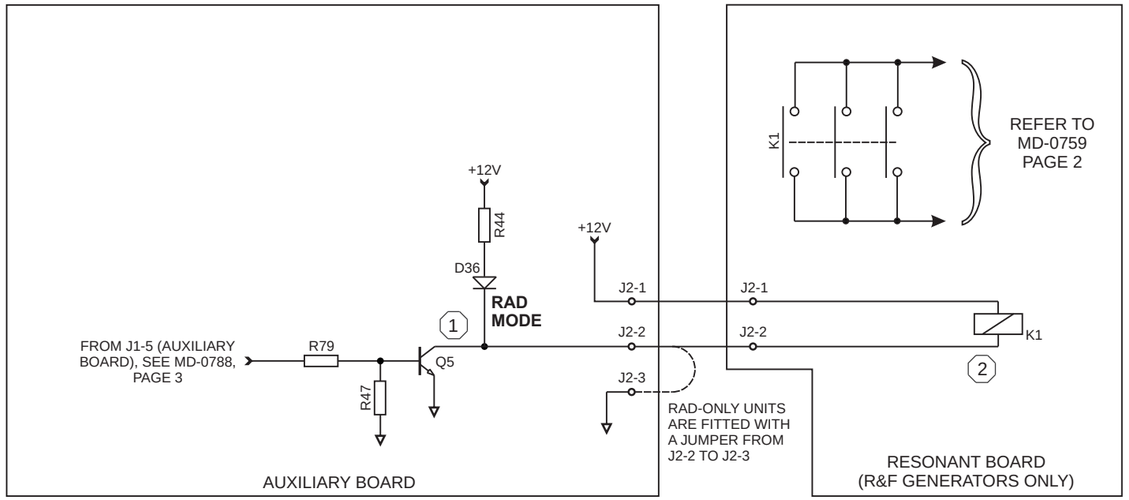
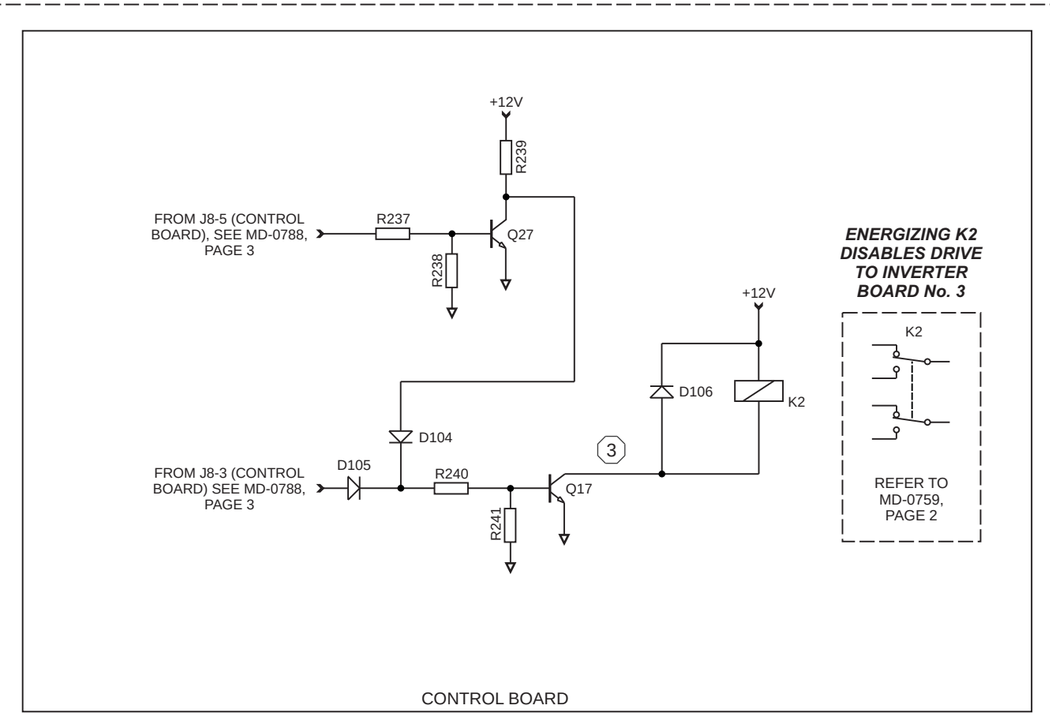


FLUORO CONTACTOR DRIVE CIRCUITS APPLICABLE TO R&F GENERATORS ONLY

NOTE REFERENCE	REMARKS
1	D36 LIT INDICATES RAD OR PULSED FLUORO MODE. D36 NOT LIT INDICATES CONTINUOUS FLUORO MODE.
2	“LOW” (APPROXIMATELY 0 VDC) = K1 ON RESONANT BOARD ENERGIZED IN RAD / PULSED FLUORO MODE. “HIGH” (APPROXIMATELY 12 VDC) = K1 ON RESONANT BOARD DE-ENERGIZED IN CONTINUOUS FLUORO MODE.
3	“LOW” (APPROXIMATELY 0 VDC) = K1 ON POWER MODE SELECT BOARD ENERGIZED IN FLUORO OR LOW POWER RAD MODE (< 20 kW APPROX). “HIGH” (APPROXIMATELY 12 VDC) = K1 ON POWER MODE SELECT BOARD DE-ENERGIZED IN HIGH POWER RAD MODE (> 20kW APPROX).



THE POWER-MODE SELECT CIRCUIT IS USED ON 80 AND 100 KW GENERATORS ONLY

DRAWN G. SANWALD	DATE 21 MAR 2000	RAD / FLUORO AND POWER MODE SELECT
CHECKED _____	_____	
DES.\MFG.\AUTH. HTW	21 MAR 2000	MD-0786 REV E
		SHEET 1 OF 1

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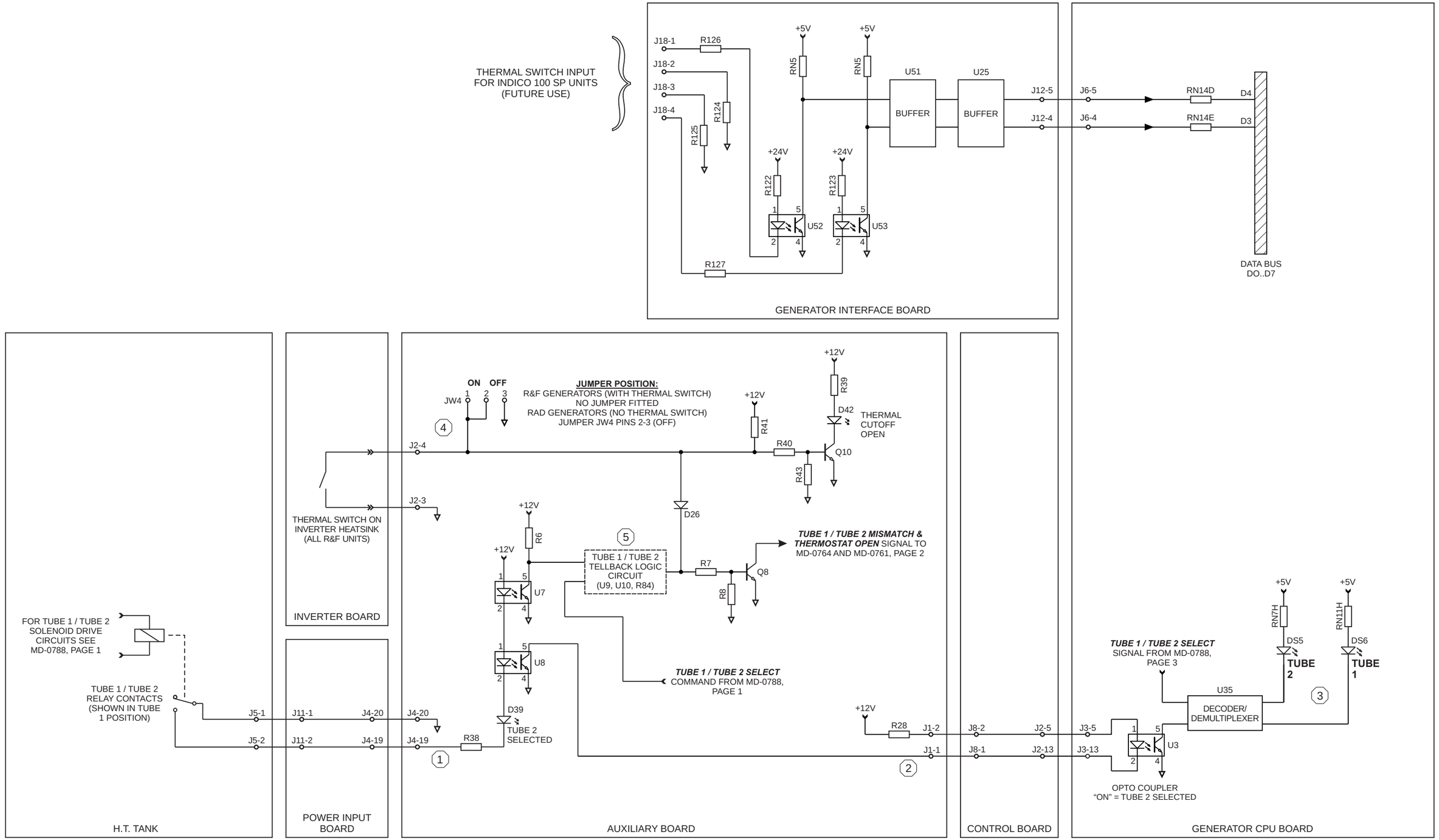


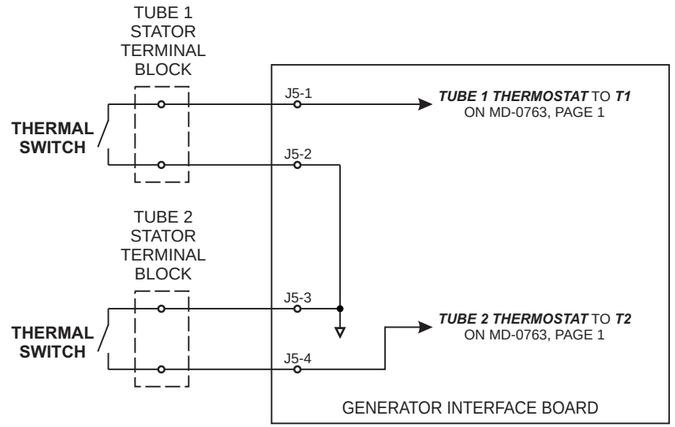
REFER TO MD-0763 (ROOM INTERFACE) FOR INTERLOCKS ACCESSED VIA THE ROOM INTERFACE BOARD

REFER TO PAGE 2 FOR TUBE THERMAL SWITCH CONNECTIONS AT THE STATOR TERMINAL BLOCK

DRAWN G. SANWALD	DATE 18 MAY 2000	**INTERLOCKS & TUBE 1 / TUBE 2 TELLBACK**
CHECKED S. BLAKE	18 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	18 MAY 2000	**MD-0787 REV G**
		SHEET 1 OF 2

Use and disclosure is subject to the restrictions on the title page of this CPI document.

NOTE REFERENCE	REMARKS
1	“LOW” (APPROXIMATELY 0 VDC) = TUBE 2 SELECTED, “HIGH” (APPROXIMATELY 10 VDC) = TUBE 1 SELECTED.
2	“LOW” (APPROXIMATELY 0 VDC) = TUBE 2 SELECTED, “HIGH” (APPROXIMATELY 12 VDC) = TUBE 1 SELECTED.
3	DS6 LIT INDICATES TUBE 1 SELECTED. DS5 LIT INDICATES TUBE 2 SELECTED. NEITHER LED LIT INDICATES A MISMATCH BETWEEN THE TUBE THAT HAS BEEN REQUESTED, AND THE TUBE THAT HAS ACTUALLY BEEN SELECTED (SEE # 5).
4	“LOW” (APPROXIMATELY 0 VDC) = INVERTER THERMAL SWITCH CLOSED (OR JUMPERED VIA JW4), “HIGH” (APPROXIMATELY 12 VDC) = INVERTER THERMAL SWITCH OPEN, OR JW4 JUMPER OMITTED ON RAD GENERATORS.
5	***THE TUBE 1 / TUBE 2 TELLBACK LOGIC CIRCUIT*** ENSURES THAT THE TUBE ACTUALLY SELECTED MATCHES THE TUBE THAT WAS REQUESTED. FOR EXAMPLE, IF TUBE 2 WAS REQUESTED BY THE CONSOLE BUT TUBE 1 WAS ACTUALLY SELECTED BY THE H.T. TANK, THE LOGIC CIRCUIT WILL INDICATE A FAULT CONDITION.



DRAWN G. SANWALD	DATE 18 MAY 2000	INTERLOCKS & TUBE 1 / TUBE 2 TELLBACK
CHECKED S. BLAKE	18 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	18 MAY 2000	MD-0787 REV G
		SHEET 2 OF 2

Use and disclosure is subject to the restrictions on the title page of this CPI document.

REFER TO PAGE 10 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY HEXAGONAL SYMBOL: ⬡

GAIN CONTROL SIGNAL FROM MD-0758 ——— (NOT USED AT THIS TIME)

+24V +12V J10-13 J10-19 J10-16 J10-11 -24V -12V

D0 RN14H J6-1 J12-1
D1 RN14G J6-2 J12-2
D2 RN14F J6-3 J12-3
D3 RN14E J6-4 J12-4
D4 RN14D J6-5 J12-5
D5 RN14C J6-6 J12-6
D6 RN14B J6-7 J12-7
D7 RN14A J6-8 J12-8

U25, U23 BUFFER & DATA LATCH: 8 7 6 5 4 3 2 1
U33 DRIVER: 11 12 13 14 15 16 17 18

4 CH 4 SELECT J10-2
4 CH 3 SELECT J10-3
4 CH 2 SELECT J10-4
4 CH 1 SELECT J10-5
5 "R" FIELD SELECT J10-7
5 "M" FIELD SELECT J10-8
5 "L" FIELD SELECT J10-9
7 START J10-6

CONTINUED ON FOLLOWING PAGES

U28 CPU — 8 9 10 U45C — R100 — J7-19 — J11-19

1 TP10

+5V R88 R87 Q6

+5V R99 Q5 R86 6 PTSTOP J10-1 R85

2 TP9 TP12 R44 R42

U37 A/D CONVERTER — 8 9 10 U23C — J7-4 — RN5B — J11-4

TP11 2 PTRAMP J10-15

3 TP12 J11-1 PTREF J10-10

J10-17

3 TP4 R30

U18 D/A CONVERTER — 9 10 8 U14C — J7-1

U46 4 5 2 1

+12V R89 Q7

R117 R116

J14-6 J14-7 J14-14 J14-3 J14-1 J14-2 J14-4 J14-12 J14-13 J14-15 J14-8 J14-9 J14-10 J14-11 -12V

DATA BUS DO..D7

GENERATOR CPU BOARD

GENERATOR INTERFACE BOARD

THIS INTERFACE NO LONGER USED

DRAWN G. SANWALD	DATE 02 JUN 2000	AEC
CHECKED _____	_____	
DES.\MFG.\AUTH. L. FOSKIN	02 JUN 2000	MD-0757 REV J
		SHEET 1 OF 10

Use and disclosure is subject to the restrictions on the title page of this CPI document.

FROM PAGE 1

GENERATOR INTERFACE BOARD

AEC BOARD

CHAMBER 4 SELECT
CHAMBER 3 SELECT
CHAMBER 2 SELECT
CHAMBER 1 SELECT
START
RIGHT FIELD SELECT
MIDDLE FIELD SELECT
LEFT FIELD SELECT
PT RAMP
PT REF
PT STOP

+12V RN6B DS5 · RN6A DS1 · RN6C DS2 · RN6D DS3 · RN6E DS4

D6 RN4A U3C → CH 4
D5 RN3D U3B → CH 3
D12 RN3C U3F → CH 2
D4 RN3A U3D → CH 1
D11 RN3B U3E U3A → STRT

+12V +24V D16 Q1 * → START

+12V +24V D30 Q2 * → RIGHT
+12V +24V D40 Q3 * → MIDDLE
+12V +24V D65 Q4 * → LEFT

TP18 J10-19 J5-19 → +24V
TP23 J10-13 J5-13 → +12V; J10-17 J5-17 → TP5 TP6 TP7
TP4 J10-11 J5-11 → -12V
TP21 J10-16 J5-16 → -24V
TP3 3 J10-15 J5-15 R54 → PT RAMP
J10-10 J5-10 RN4C → PT REF
J10-1 J5-1 → PT STOP

+12V RN4D D27 R56 D22 U6 RN4B

TP17 2 U4B U4A C11
TP20 8 S4 STRT R32 * C4
CH 1 S3A R53 R11
CH 2 S3B R12
CH 3 S3C R13
CH 4 S3D R14
U2B
R1 S2A CH 1
R2 S2B CH 2
R3 S2C CH 3
R4 S2D CH 4
TP19 9 U2A
TP2 10 U1A
STRT SAMPLE & HOLD

12 TP22 +12V
+500V TP10
TP24 +/-300V
TP9 R66 +45V
SET VALUE R79 11
CONVERTER CIRCUIT 12 VDC TO 45 VDC AND +/-300 / +500 VDC
INCLUDES U7 AND T1
* H.V.

AEC CH 1

LEFT JW8 1 2 3 RIGHT
JW7 1 2 3
TP11 13 R89 CH 1 S1D R90

+/-300V	J1-2	+/-300 V
H.V.	J11-1 J1-1	+/-300/+500 V
+45V	J1-3	+45 V
START	J11-4 J1-8	RESET/START
MIDDLE	J11-3 J1-10	M FIELD SEL
L/R	J11-2 J1-9	R FIELD SEL
R/L	J11-6 J1-11	L FIELD SEL
	J11-5 J1-12	CHAMBER O/P
	J11-9 J1-7	GROUND

AEC CH 2

LEFT JW6 1 2 3 RIGHT
JW5 1 2 3
TP12 13 R67 CH 2 S1C R68

+/-300V	J2-2	+/-300 V
H.V.	J12-1 J2-1	+/-300/+500 V
+45V	J2-3	+45 V
START	J12-4 J2-8	RESET/START
MIDDLE	J12-3 J2-10	M FIELD SEL
L/R	J12-2 J2-9	R FIELD SEL
R/L	J12-6 J2-11	L FIELD SEL
	J12-5 J2-12	CHAMBER O/P
	J12-9 J2-7	GROUND

AEC CH 3

LEFT JW4 1 2 3 RIGHT
JW3 1 2 3
TP13 13 R57 CH 3 S1B R58

+/-300V	J3-2	+/-300 V
H.V.	J13-1 J3-1	+/-300/+500 V
+45V	J3-3	+45 V
START	J13-4 J3-8	RESET/START
MIDDLE	J13-3 J3-10	M FIELD SEL
L/R	J13-2 J3-9	R FIELD SEL
R/L	J13-6 J3-11	L FIELD SEL
	J13-5 J3-12	CHAMBER O/P
	J13-9 J3-7	GROUND

AEC CH 4

LEFT JW2 1 2 3 RIGHT
JW1 1 2 3
TP14 13 R35 CH 4 S1A R36

+/-300V	J4-2	+/-300 V
H.V.	J14-1 J4-1	+/-300/+500 V
+45V	J4-3	+45 V
START	J14-4 J4-8	RESET/START
MIDDLE	J14-3 J4-10	M FIELD SEL
L/R	J14-2 J4-9	R FIELD SEL
R/L	J14-6 J4-11	L FIELD SEL
	J14-5 J4-12	CHAMBER O/P
	J14-9 J4-7	GROUND

THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 734614

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

THE -24V OUTPUTS ON J1 TO J4 AND THE +/- 12V OUTPUTS ON J1 TO J4 AND J11 TO J14 ARE NOT SHOWN ON THIS DIAGRAM. THESE ARE DETAILED ON THE CONNECTOR PIN OUT TABLES IN CHAPTER 3D.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL.

DESIGNATES A FACTORY CONFIGURED LOGIC OR SIGNAL LEVEL. AEC BOARDS ARE CONFIGURED AT THE TIME OF ORDER TO BE COMPATIBLE WITH THE SPECIFIED AEC CHAMBER(S). FOR EXAMPLE, THE **START** SIGNAL TO THE CHAMBER MAY BE FACTORY CONFIGURED TO BE ACTIVE LOW (0 V), ACTIVE HIGH +12 V, OR ACTIVE HIGH +24 V.

DRAWN G. SANWALD	DATE 02 JUN 2000	AEC
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DES.\MFG.\AUTH. L. FOSKIN	02 JUN 2000	MD-0757 REV J
		SHEET 2 OF 10

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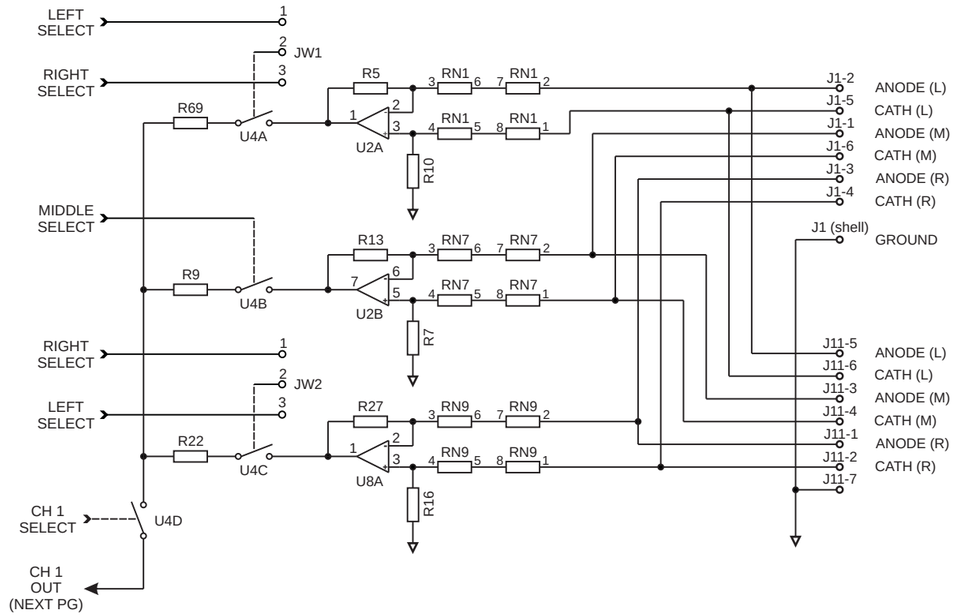
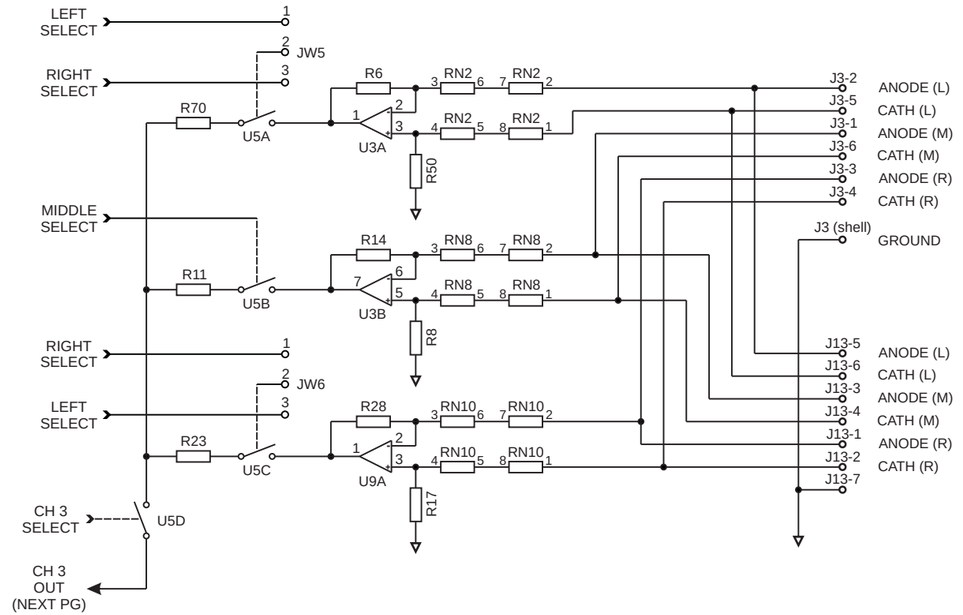
AEC CH 1



AEC CH 3



AEC CH 2

AEC CH 4

THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 737992. THIS PAGE SHOWS THE INPUT CIRCUITS; THE SIGNAL PROCESSING CIRCUITS ARE CONTINUED ON THE NEXT PAGE.

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL (0V = OFF, 5V = ON).

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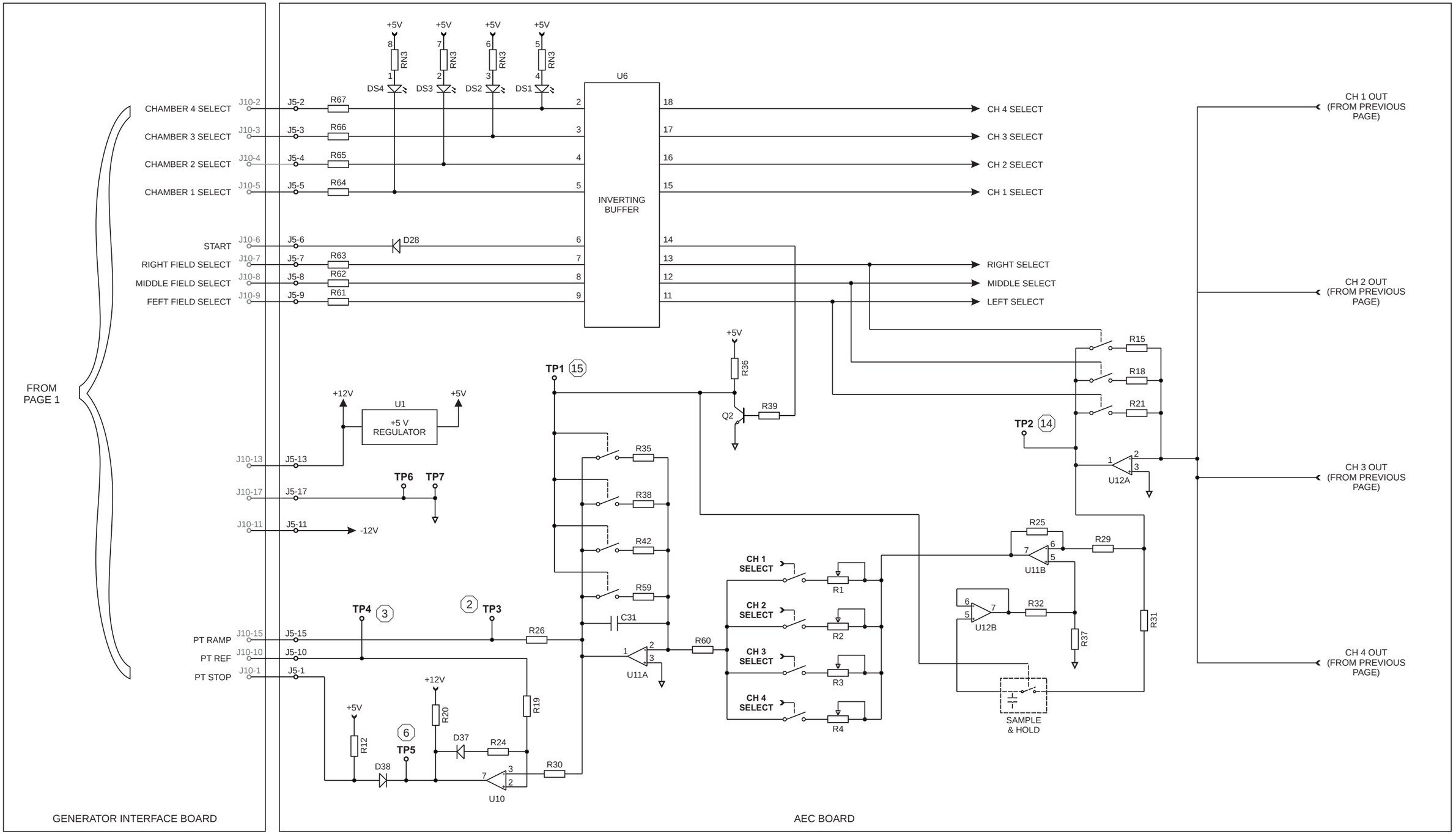

THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 737992. THIS PAGE SHOWS THE SIGNAL PROCESSING CIRCUITS; THE INPUT CIRCUITS ARE SHOWN ON THE PREVIOUS PAGE.

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL (0V = OFF, 5V = ON).

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		SHEET 4 OF 10

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FROM PAGE 1

CHAMBER 4 SELECT — J10-2 — J5-2 — R61
CHAMBER 3 SELECT — J10-3 — J5-3 — R62
CHAMBER 2 SELECT — J10-4 — J5-4 — R63
CHAMBER 1 SELECT — J10-5 — J5-5 — R64
START — J10-6 — J5-6 — D20
RIGHT FIELD SELECT — J10-7 — J5-7 — R66
MIDDLE FIELD SELECT — J10-8 — J5-8 — R67
LEFT FIELD SELECT — J10-9 — J5-9 — R68

+5V — R49 — DS1
+5V — R50 — DS2
+5V — R51 — DS3
+5V — R52 — DS4

U6 INVERTING BUFFER

2	CHAMBER 4 SELECT	18	CH 4 SELECT
3	CHAMBER 3 SELECT	17	CH 3 SELECT
4	CHAMBER 2 SELECT	16	CH 2 SELECT
5	CHAMBER 1 SELECT	15	CH 1 SELECT
6	START	14	
7	RIGHT FIELD SELECT	13	
8	MIDDLE FIELD SELECT	12	
9	LEFT FIELD SELECT	11	

+5V — R39 — R40 — Q5 — START/
+12V — D12 — START — R38 — Q4

+12V — D11 — R37 — Q3 — LEFT SELECT
+12V — D10 — R36 — Q2 — MIDDLE SELECT
+12V — D9 — R35 — Q1 — RIGHT SELECT

+12V — U3 +5 V REGULATOR — +5V

J10-13 — J5-13
J10-17 — J5-17 — TP11 TP12
J10-11 — J5-11 — -12V

PT RAMP — J10-15 — J5-15 — TP9 (3) — TP8 (2) — R30
PT REF — J10-10 — J5-10
PT STOP — J10-1 — J5-1

+5V — R69
+12V — R34
R32
R31
(6) TP10 — D27
D25 — R33
7 — 3 — 2 — U9

TP7 (8)
U4A
START/ — *
R11 — CH 1 SELECT
R12 — CH 2 SELECT
R13 — CH 3 SELECT
R14 — CH 4 SELECT
U8B
U4B
TP6 (9)
TP5 (10)
U8A
START/
SAMPLE & HOLD
U7A

AEC CH 1

LEFT SELECT — JW8 — RIGHT SELECT — JW7
NO CONNECTION — N/C
J1-2 — LEFT/RIGHT
J1-6 — RIGHT/LEFT
MIDDLE SELECT — J1-3 — MIDDLE
+12V — START — J1-4 — RESET/START
J1-8 — +12V
(13) TP1 — R1 — J1-5 — CHAMBER O/P
J1-7 — -12V
J1-9 — GROUND
CH 1 SELECT — U1D — R2 — -12V

AEC CH 2

LEFT SELECT — JW6 — RIGHT SELECT — JW5
NO CONNECTION — N/C
J2-2 — LEFT/RIGHT
J2-6 — RIGHT/LEFT
MIDDLE SELECT — J2-3 — MIDDLE
+12V — START — J2-4 — RESET/START
J2-8 — +12V
(13) TP2 — R3 — J2-5 — CHAMBER O/P
J2-7 — -12V
J2-9 — GROUND
CH 2 SELECT — U1C — R4 — -12V

AEC CH 3

LEFT SELECT — JW4 — RIGHT SELECT — JW3
NO CONNECTION — N/C
J3-2 — LEFT/RIGHT
J3-6 — RIGHT/LEFT
MIDDLE SELECT — J3-3 — MIDDLE
+12V — START — J3-4 — RESET/START
J3-8 — +12V
(13) TP3 — R5 — J3-5 — CHAMBER O/P
J3-7 — -12V
J3-9 — GROUND
CH 3 SELECT — U1B — R6 — -12V

AEC CH 4

LEFT SELECT — JW2 — RIGHT SELECT — JW1
NO CONNECTION — N/C
J4-2 — LEFT/RIGHT
J4-6 — RIGHT/LEFT
MIDDLE SELECT — J4-3 — MIDDLE
+12V — START — J4-4 — RESET/START
J4-8 — +12V
(13) TP4 — R7 — J4-5 — CHAMBER O/P
J4-7 — -12V
J4-9 — GROUND
CH 4 SELECT — U1A — R8 — -12V

GENERATOR INTERFACE BOARD

AEC BOARD

THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 737998

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL.

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DES.\MFG.\AUTH. L. FOSKIN	02 JUN 2000	MD-0757 REV J
		SHEET 5 OF 10

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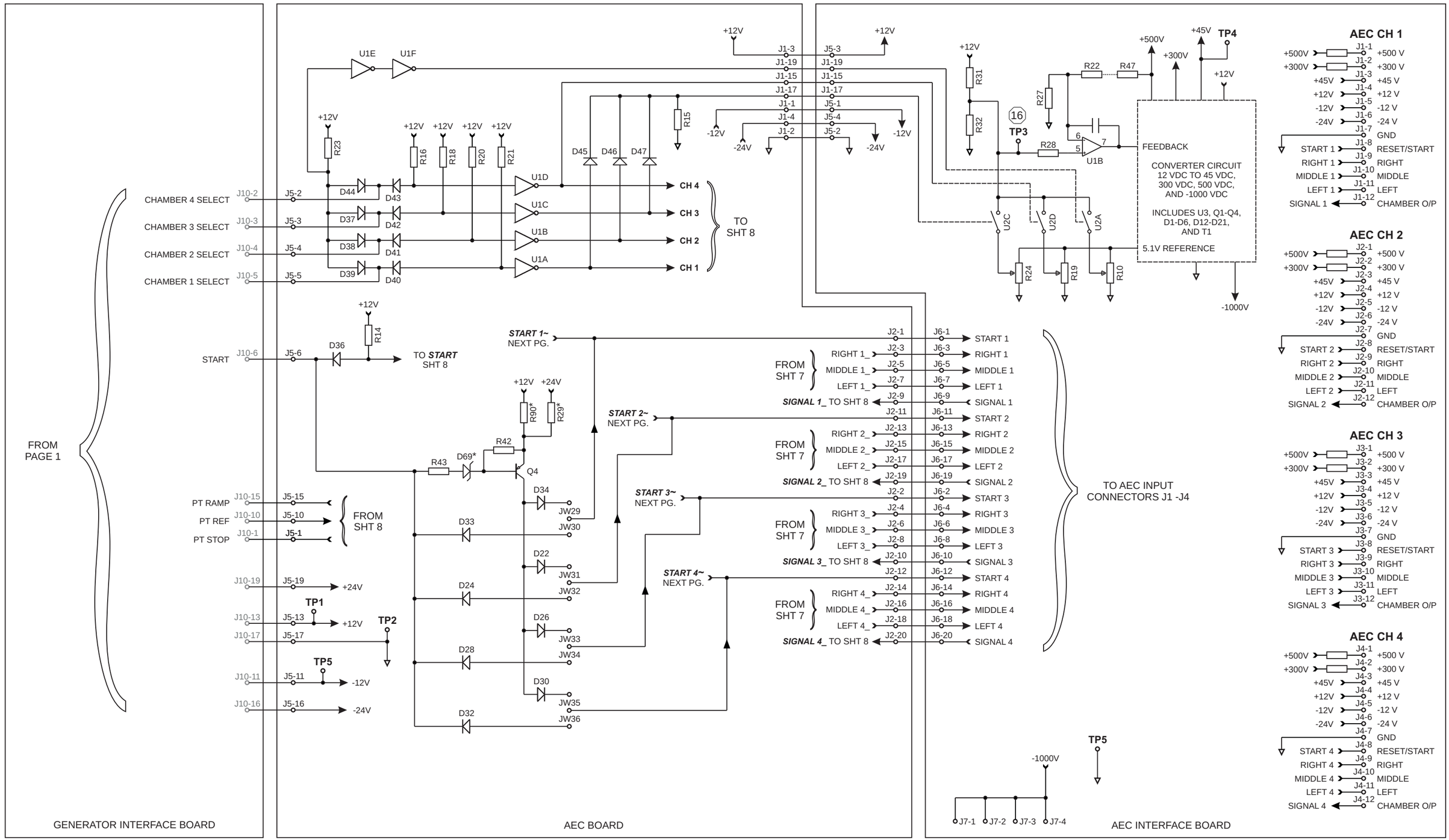

THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 734654, WHICH CONSISTS OF AEC INTERFACE BOARD 728399 AND AEC BOARD 734630. THE AEC BOARD CIRCUITS ARE CONTINUED ON PAGES 7 AND 8.

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. "SWITCHES" THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL.

* NOT FITTED ON ALL MODELS. REFER TO SUP734654 IN THE FRONT OF THIS MANUAL FOR DETAILS

DRAWN G. SANWALD	DATE 02 JUN 2000	AEC
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DES.\MFG.\AUTH. L. FOSKIN	02 JUN 2000	MD-0757 REV J
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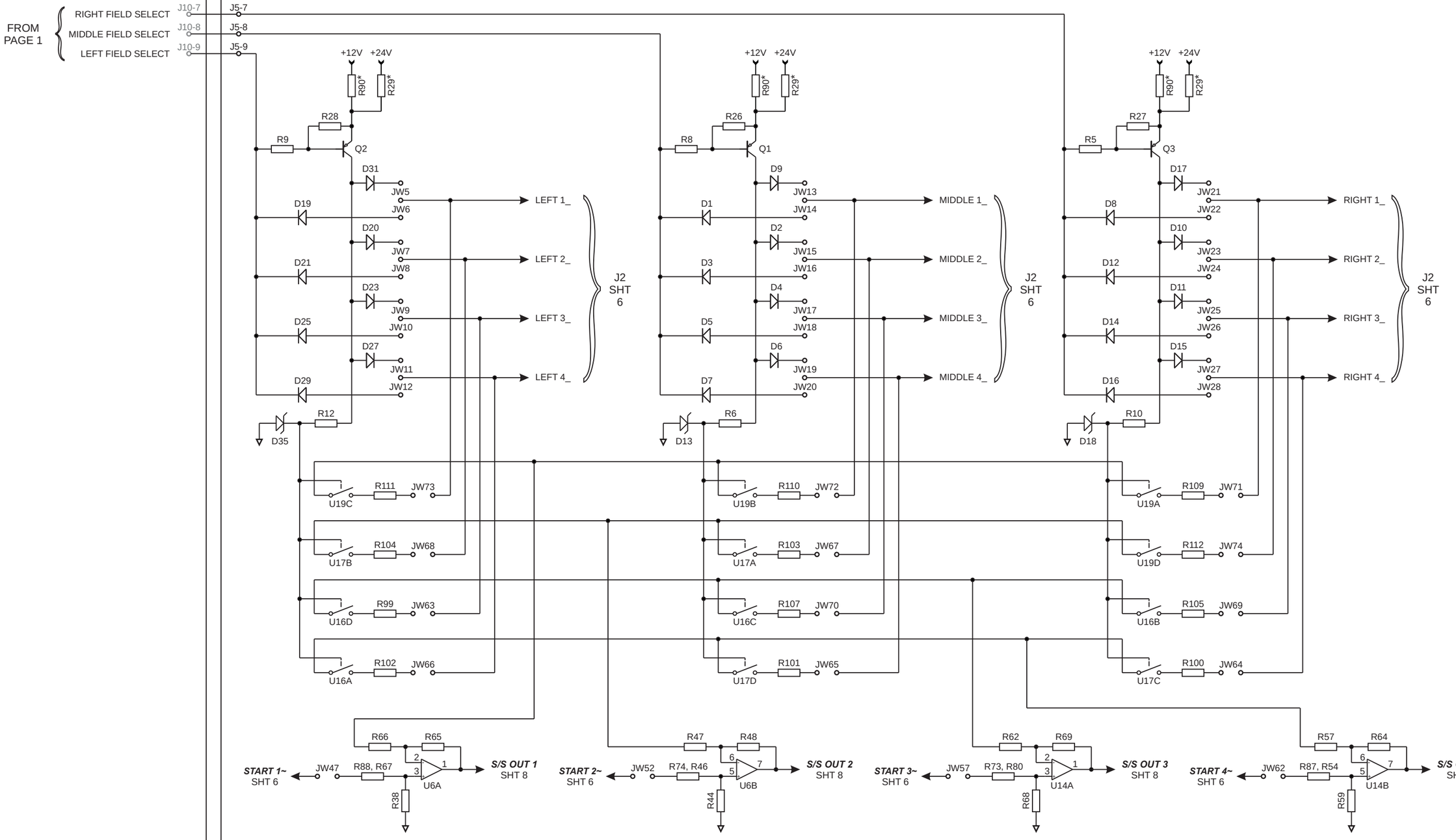

THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 734654, WHICH CONSISTS OF AEC INTERFACE BOARD 728399 AND AEC BOARD 734630. THE AEC BOARD CIRCUITS ARE CONTINUED ON PAGES 6 AND 8.

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL.

* NOT FITTED ON ALL MODELS. REFER TO SUP734654 IN THE FRONT OF THIS MANUAL FOR DETAILS

DRAWN G. SANWALD	DATE 02 JUN 2000	AEC
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DES.\MFG.\AUTH. L. FOSKIN	02 JUN 2000	MD-0757 REV J
		SHEET 7 OF 10

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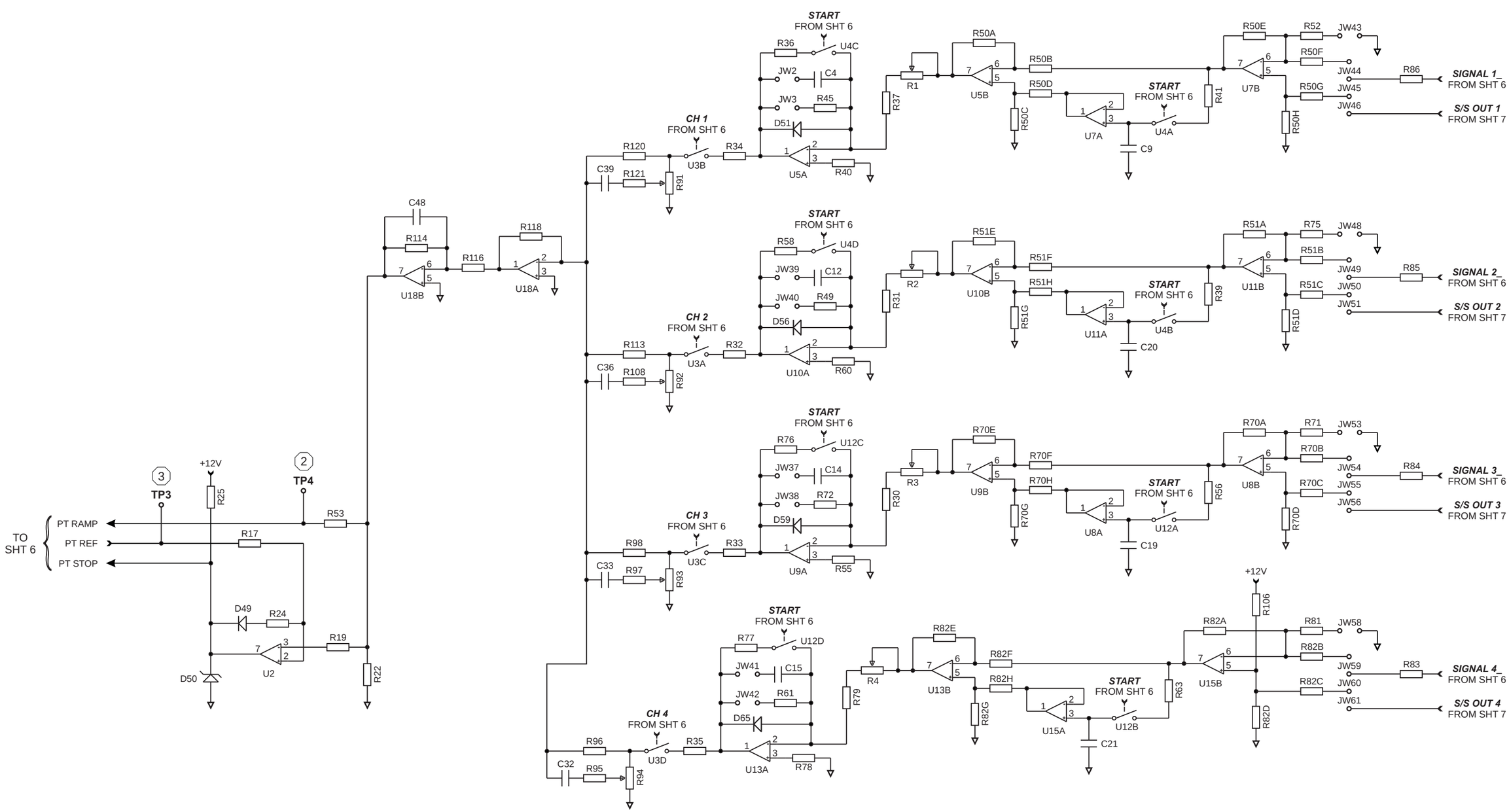

THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 734654, WHICH CONSISTS OF AEC INTERFACE BOARD 728399 AND AEC BOARD 734630. THE AEC BOARD CIRCUITS ARE CONTINUED ON PAGES 8 AND 9.

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL (0V = OFF, 12V = ON).

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DES.\MFG.\AUTH. L. FOSKIN	02 JUN 2000	MD-0757 REV J
		SHEET 8 OF 10

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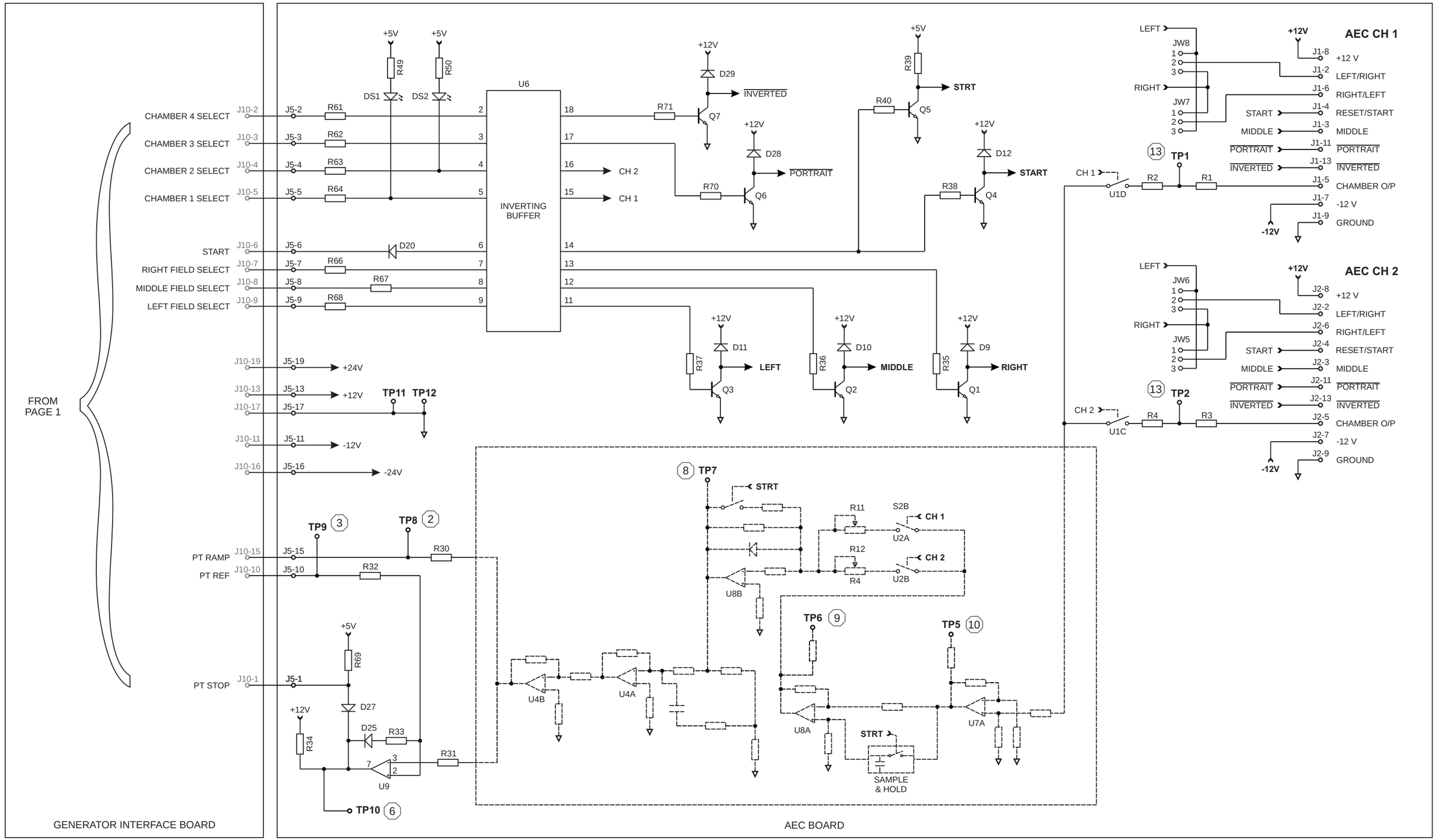

THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 739389

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL.

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DES.\MFG.\AUTH. L. FOSKIN	02 JUN 2000	MD-0757 REV J
		SHEET 9 OF 10

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NOTE REFERENCE	REMARKS
1	“HIGH” (APPROXIMATELY 5 VDC) = NO $\overline{\text{PTSTOP}}$ (PHOTOTIMER STOP) SIGNAL RECEIVED FROM AEC BOARD. “LOW” (APPOXIMATELY 0 VDC) = $\overline{\text{PTSTOP}}$ SIGNAL RECEIVED FROM AEC BOARD.
2	AEC RAMP. THIS IS A SIGNAL RAMPING FROM 0 TOWARD +10 VDC. THE ACTUAL MAGNITUDE WILL DEPEND ON THE AEC TECHNIQUE.
3	AEC REFERENCE VOLTAGE, 0 TO +10 VDC, DEPENDING ON AEC TECHNIQUE. THE LENGTH OF THE AEC EXPOSURE IS PROPORTIONAL TO THE AEC REFERENCE VOLTAGE.
4	“HIGH” (> 10 VDC) = AEC CHANNEL DESELECTED, “LOW” (APPROXIMATELY 0 VDC) = AEC CHANNEL SELECTED.
5	“HIGH” (> 10 VDC) = L, M, R, FIELD DESELECTED, “LOW” (APPROXIMATELY 0 VDC) = L, M, R, FIELD SELECTED.
6	“HIGH” (> 10 VDC) = NO AEC STOP REQUEST (INSUFFICIENT RAMP TO TERMINATE AEC EXPOSURE), “LOW” (APPROXIMATELY 0 VDC) = AEC STOP REQUESTED (AEC EXPOSURE TERMINATED).
7	“HIGH” (> 10 VDC) = AEC START NOT REQUESTED, “LOW” (APPROXIMATELY 0 VDC) = AEC START REQUESTED.
8	THE VOLTAGE AND MAGNITUDE OF THE RAMP AT THIS POINT SHOULD BE APPROXIMATELY THE SAME AS THE **PT RAMP** OUTPUT, NOTE REFERENCE 2 .
9	THIS WILL BE A NEGATIVE DC VOLTAGE OR RAMP, DEPENDING ON AEC CHAMBER OUTPUT. THE MAGNITUDE OF THE DC VOLTAGE OR RAMP IS DEPENDENT ON THE AEC TECHNIQUE IN USE.
10	THIS WILL BE A POSITIVE DC VOLTAGE OR RAMP, DEPENDING ON AEC CHAMBER OUTPUT. THE MAGNITUDE OF THE DC VOLTAGE OR RAMP IS DEPENDENT ON THE AEC TECHNIQUE IN USE.
11	R79 ADJUSTS THE +45V, +300V, AND +500V OUTPUTS FROM THE DC TO DC CONVERTER CIRCUIT. REFER TO CHAPTER 3D FOR DETAILS.
12	THE VOLTAGE AT TP22 SHOULD BE APPROXIMATELY AS SHOWN IN FIGURE 1 (BELOW). THE MAXIMUM DUTY CYCLE WILL BE APPROXIMATELY 45%, DEPENDING ON THE LOAD ON THE HV SUPPLIES.
13	THE VOLTAGE AT THIS TEST POINT IS THE OUTPUT OF THE AEC CHAMBER. REFER TO THE AEC CHAMBER MANUFACTURERS DOCUMENTATION FOR DETAILS.
14	THIS WILL BE A POSITIVE DC VOLTAGE. THE MAGNITUDE OF THE DC VOLTAGE IS DEPENDENT ON THE AEC TECHNIQUE IN USE.
15	THIS IS THE START SIGNAL. “HIGH” (5 VDC) = $\overline{\text{START}}$ = ANALOG SWITCHES CLOSED, “LOW” (0 VDC) = START = ANALOG SWITCHES OPEN.
16	THIS WILL BE A VOLTAGE BETWEEN 0 AND 5.1 V, DEPENDING ON THE SETTING OF THE ACTIVE POTENTIOMETER R10, R19, OR R24..

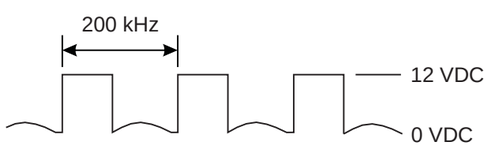

FIGURE 1

DRAWN G. SANWALD	DATE 02 JUN 2000	AEC
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		SHEET 10 OF 10

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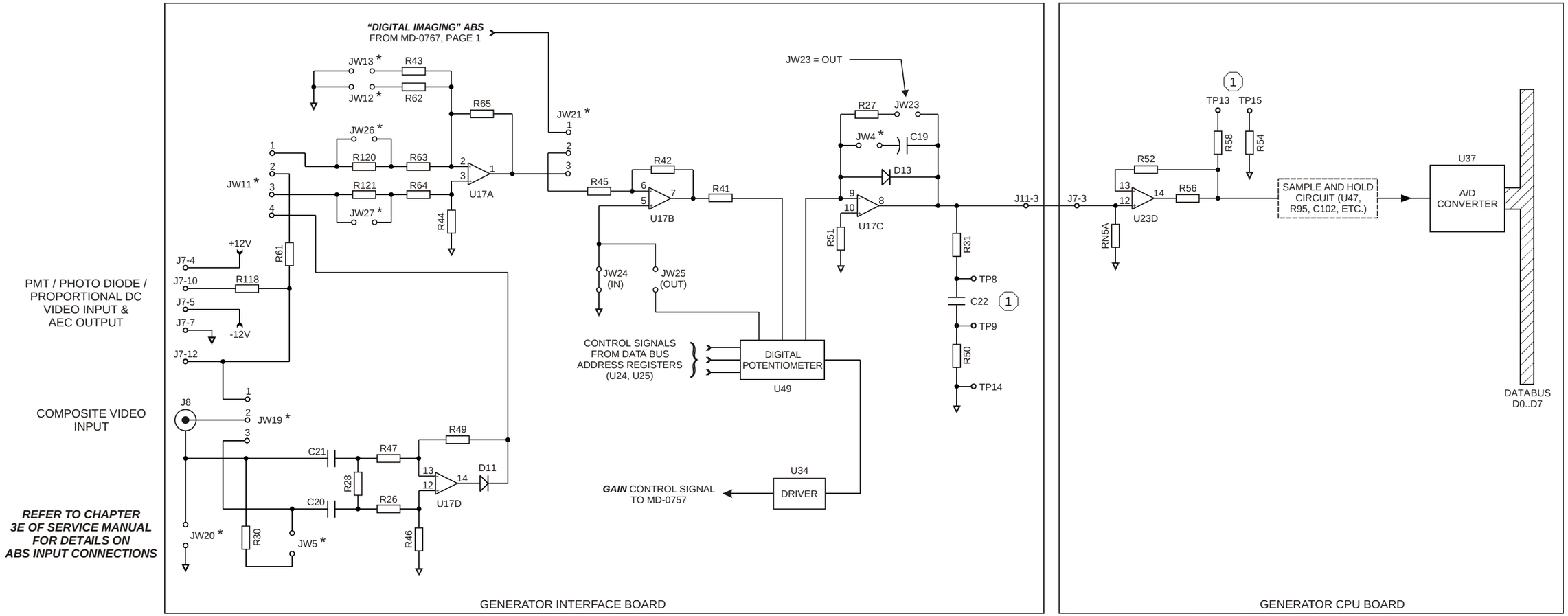

* REFER TO CHAPTER 3E OF SERVICE MANUAL TO DETERMINE REQUIRED JUMPER POSITIONS FOR THESE CONNECTORS.

NOTE REFERENCE	REMARKS
1	A DC VOLTAGE WILL BE PRESENT FROM TP8 (TO TP9 OR GROUND), AND FROM TP13 TO TP15 WHEN OPERATING WITH **ABS** ON. THIS VOLTAGE WILL TYPICALLY RANGE FROM 0.5 TO 5 VDC, AND WILL VARY DEPENDING ON THE **NOMINAL DOSE** VALUE IN THE ***ABS SETUP*** MENU.

DRAWN G. SANWALD	DATE 16 MAY 2000	**ABS (AUTOMATIC BRIGHTNESS STABILIZATION)**
CHECKED KVR	16 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	16 MAY 2000	**MD-0758 REV E**
		SHEET 1 OF 1

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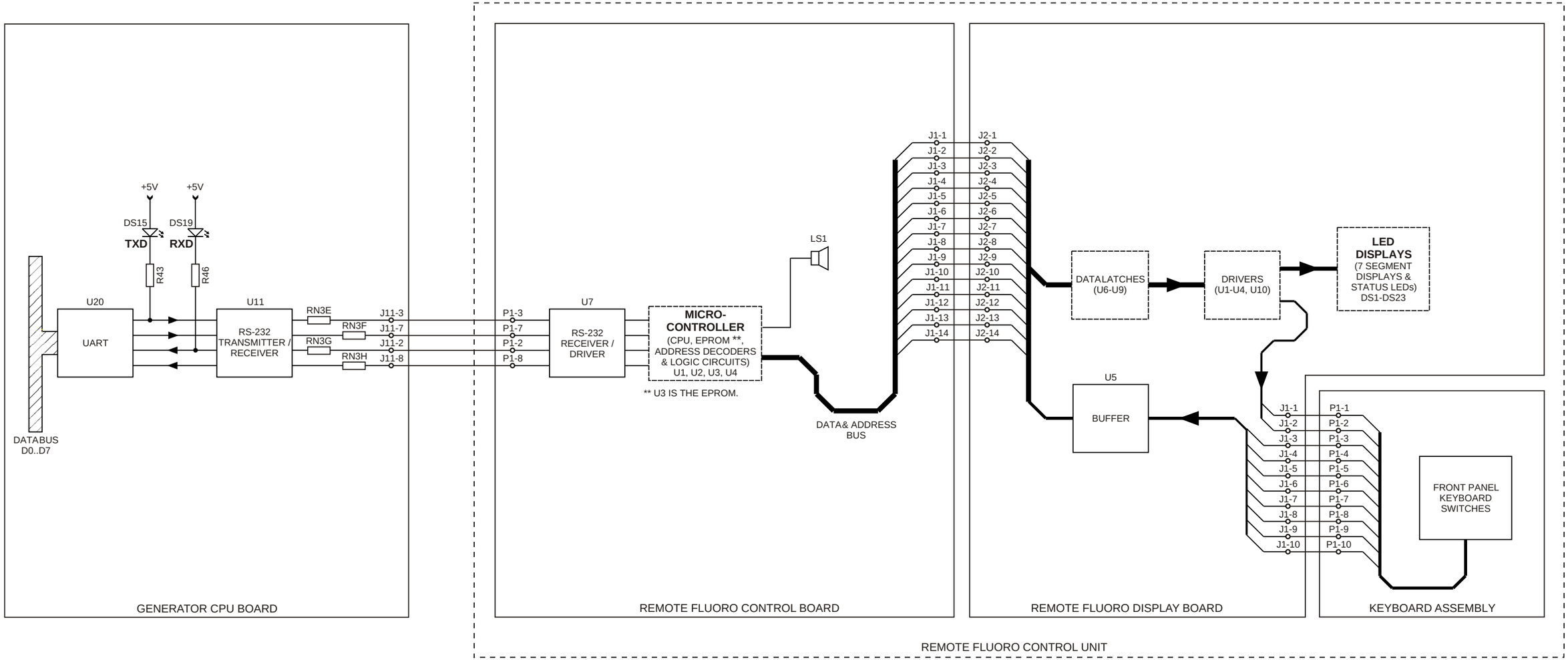

LIMITED TROUBLESHOOTING CAN BE PERFORMED ON THE **REMOTE FLUORO CONTROL** ASSEMBLY IN THE FIELD. THE DC RAILS CAN BE CHECKED (REFER TO MD-0788), AND THE **TXD** AND **RXD** LEDs ON THE GENERATOR CPU BOARD MAY BE OBSERVED (THESE WILL FLASH ON AND OFF TO INDICATE DATA FLOW). MEANINGFUL MEASUREMENTS CANNOT BE MADE ON COMMUNICATIONS, DATA, AND CONTROL LINES.

DRAWN G. SANWALD	DATE 02 JUN 2000	**REMOTE FLUORO CONTROL**
CHECKED _____	_____	
DES.\MFG.\AUTH. L. FOSKIN	02 JUN 2000	**MD-0766 REV D**
		SHEET 1 OF 1

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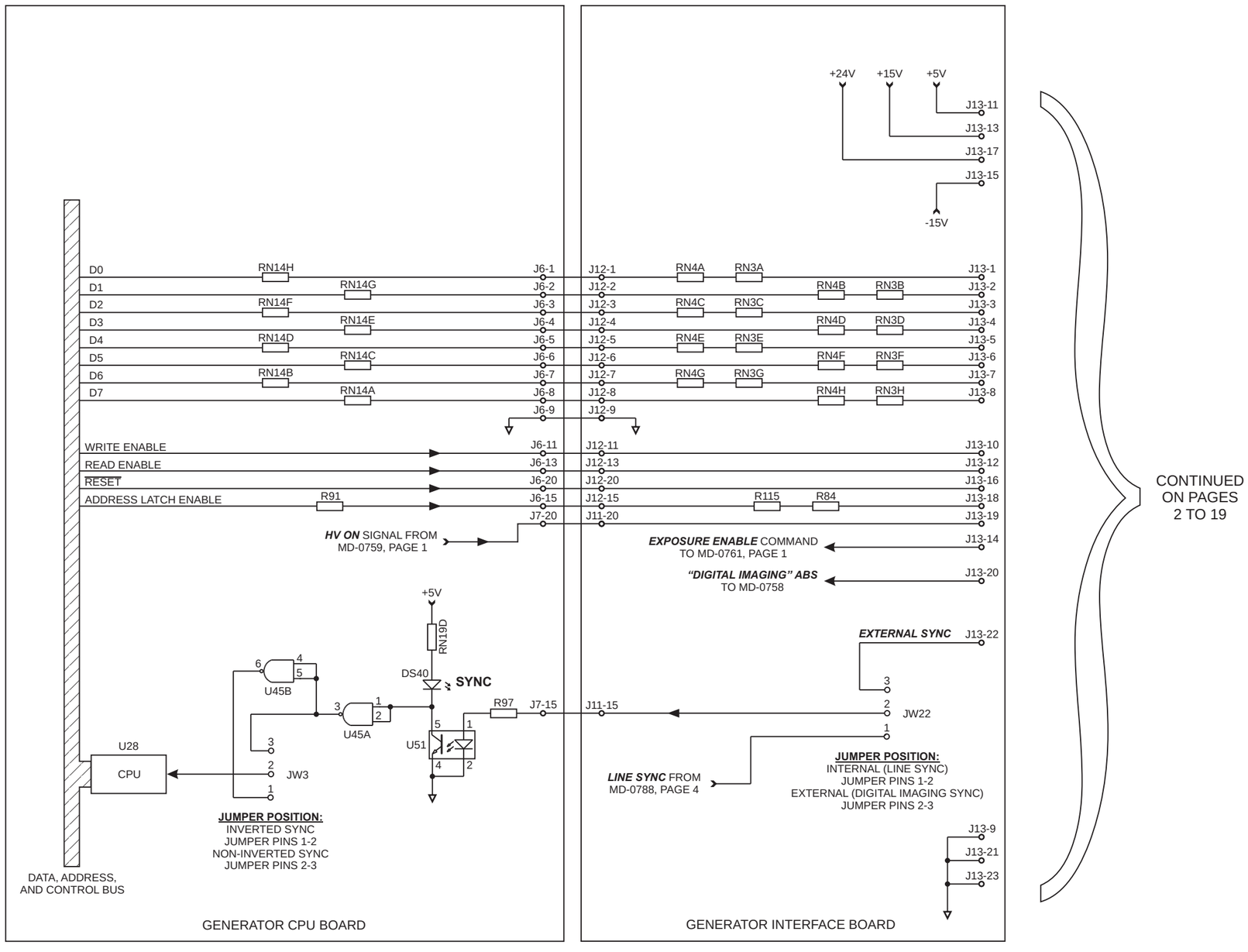

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CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	MD-0767 REV M
		SHEET 1 OF 19

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FROM PAGE 1

+5V +15V +24V

J1-11
J1-13
J1-17
J1-15
-15V

J1-20

J1-14

J1-19

U3B

JW1

J1-1
J1-2
J1-3
J1-4
J1-5
J1-6
J1-7
J1-8
J1-10
J1-12
J1-16
J1-18

ADDRESS DECODER CIRCUITS (U1, U2, U3A, U6A)

J1-9
J1-21
J1-23

U4
DATA LATCH

U6
DRIVER

U7
MUX

TP1 TP2

R2 R3

R1 U10

R10 DS4 EXON
R12 DS6 PFL
R13 DS7 HCF
R14 DS8 PREP
R15 DS9 GEN READY
R16 DS10 TOMO

F1

U8
BUFFER

R6 R7 U13 DS1 OFL

U9
BUFFER

SW1

R5 R8 U12 DS2 STOP EXP.

R4 R9 U11 DS3 O.EXP

R11 U16

R17 U14

J2-20
J2-21
J2-1
J2-7
J2-3
J2-4
J2-5
J2-6
J2-22
J2-9
J2-23
J2-2
J2-10
J2-12
J2-11

J3-7
J3-1
J3-3
J3-9
J3-10
J3-5
J3-6
J3-2
J3-4
J3-8

DIGITAL I/O BOARD

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 733752.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING THE CONNECTIONS TO J2, J3.

DRAWN G. SANWALD	DATE 16 MAY 2000	DIGITAL INTERFACE
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	MD-0767 REV M
		SHEET 2 OF 19

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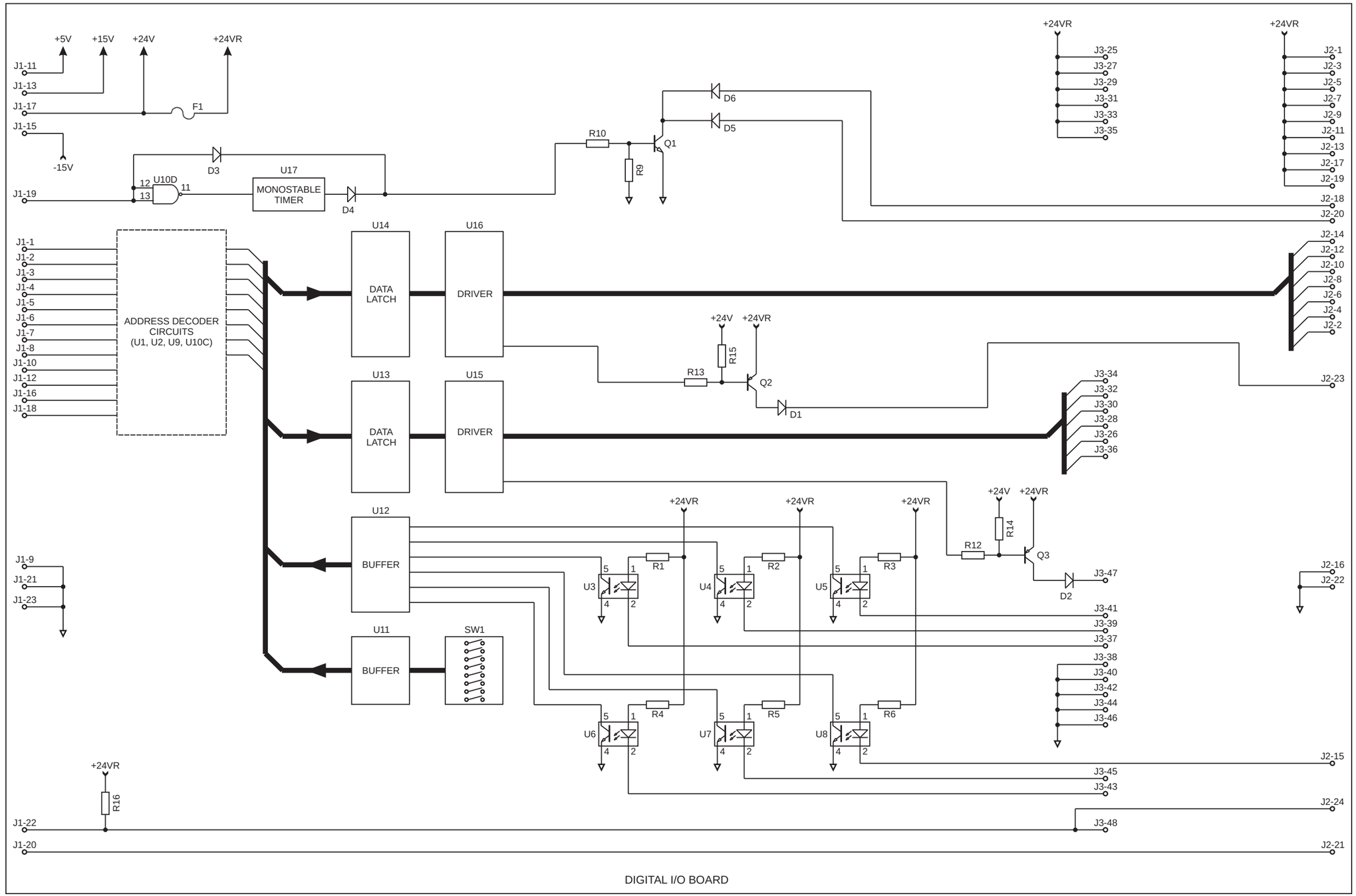
FROM PAGE 1



DIGITAL I/O BOARD

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 733947.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING THE CONNECTIONS TO J2, J3.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 3 OF 19

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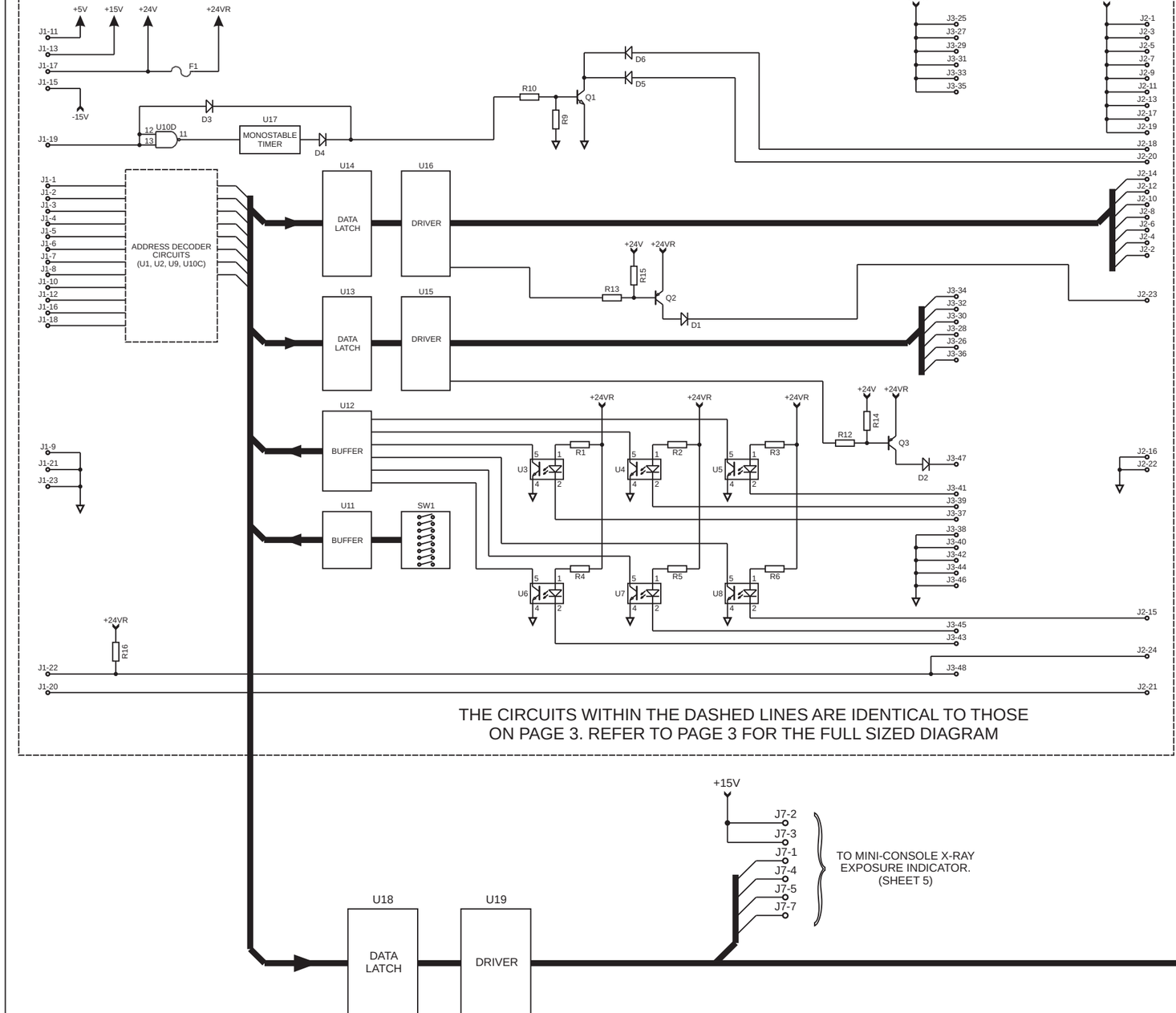
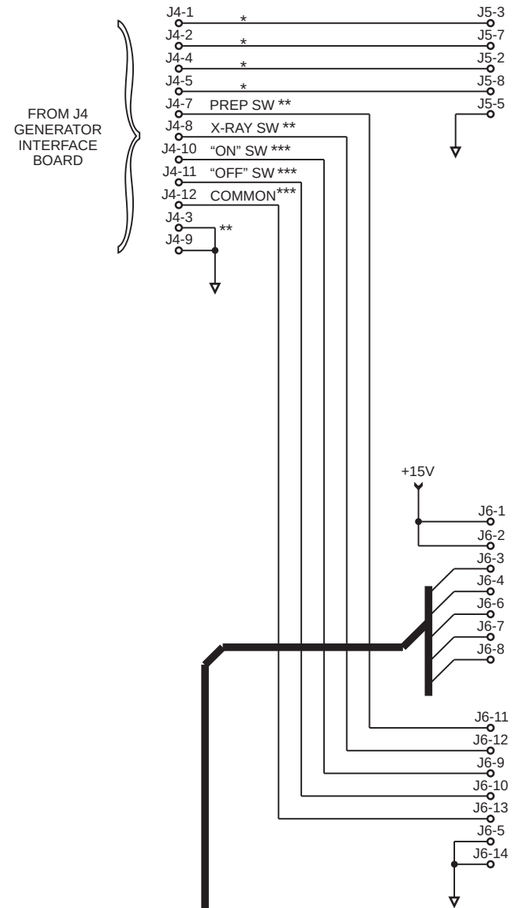
FROM PAGE 1



* THESE ARE SERIAL COMMUNICATION LINES. REFER TO MD-0829, SHEET 1, FOR THE CORRESPONDING CONNECTIONS ON THE GENERATOR INTERFACE BOARD.

** REFER TO MD-0761, SHEET 1, FOR THE PREP AND X-RAY INPUTS ON THE GENERATOR INTERFACE BOARD.

*** REFER TO MD-0762, SHEET 1, FOR THE POWER ON & OFF INPUTS ON THE GENERATOR INTERFACE BOARD.



THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 735921.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING THE CONNECTIONS TO J2, J3, J5.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 4 OF 19

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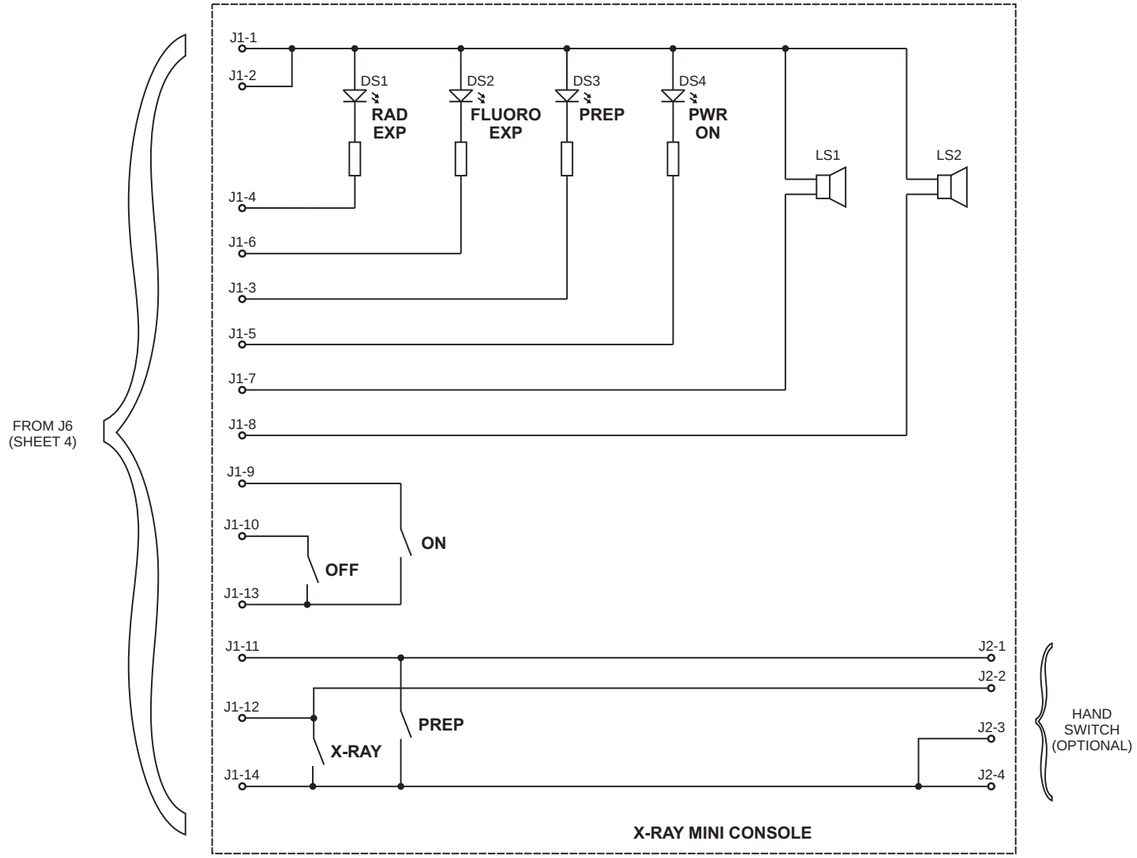

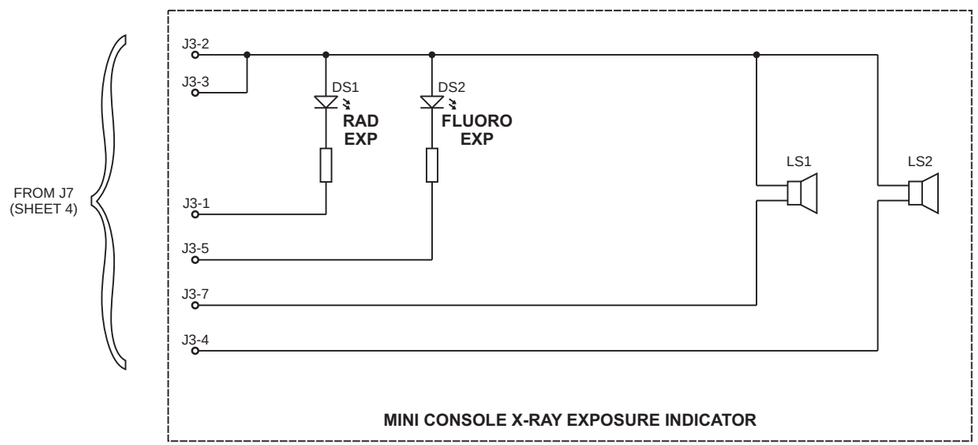

THE OPTIONAL “X-RAY MINI CONSOLE” AND OPTIONAL “MINI CONSOLE X-RAY EXPOSURE INDICATOR” ARE TYPICALLY USED WITH DIGITAL IMAGING SYSTEMS THAT HAVE INTEGRATED GENERATOR CONSOLE CONTROL FUNCTIONS.

DRAWN G. SANWALD	DATE 16 MAY 2000	DIGITAL INTERFACE
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	MD-0767 REV M
		SHEET 5 OF 19

Use and disclosure is subject to the restrictions on the title page of this CPI document.

FROM PAGE 1

+5V
+15V
+24V
+5V(A)
J1-11
J1-13
J1-17
U12
+5 V REGULATOR
F1
+24V
J2-14
J2-21

J1-1
J1-2
J1-3
J1-4
J1-5
J1-6
J1-7
J1-8
J1-10
J1-12
J1-16
J1-18
ADDRESS DECODER CIRCUITS (U1, U2, U3A, U5A)
U4
DATA LATCH
U6
DRIVER

J1-14

J1-9
J1-21
J1-23

U8
BUFFER
U9
BUFFER
SW1

+15V
GENERATOR READY
DS4
R2
U7
J2-8

+15V
EXPOSURE IN PROCESS (EIP)
DS3
R1
U10
J2-22

J2-11
J2-13

+24V
R9
R8
X-RAY
DS2
J2-15
U16
R6
R7
J2-4
J3-1
J2-5
J3-4
J2-6
J3-3
U14
J2-16
J3-10
U15
J2-18
J3-11
J2-17
J2-19
J3-12

+5V(A)
U11
EXPOSE RDY
DS5
R3
+24V
U13
J2-9
J2-12
R4
R5
DS1
PREP

DIGITAL I/O BOARD

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 735406.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING THE CONNECTIONS TO J2, J3.

DRAWN G. SANWALD	DATE 16 MAY 2000	DIGITAL INTERFACE
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	MD-0767 REV M
		SHEET 6 OF 19

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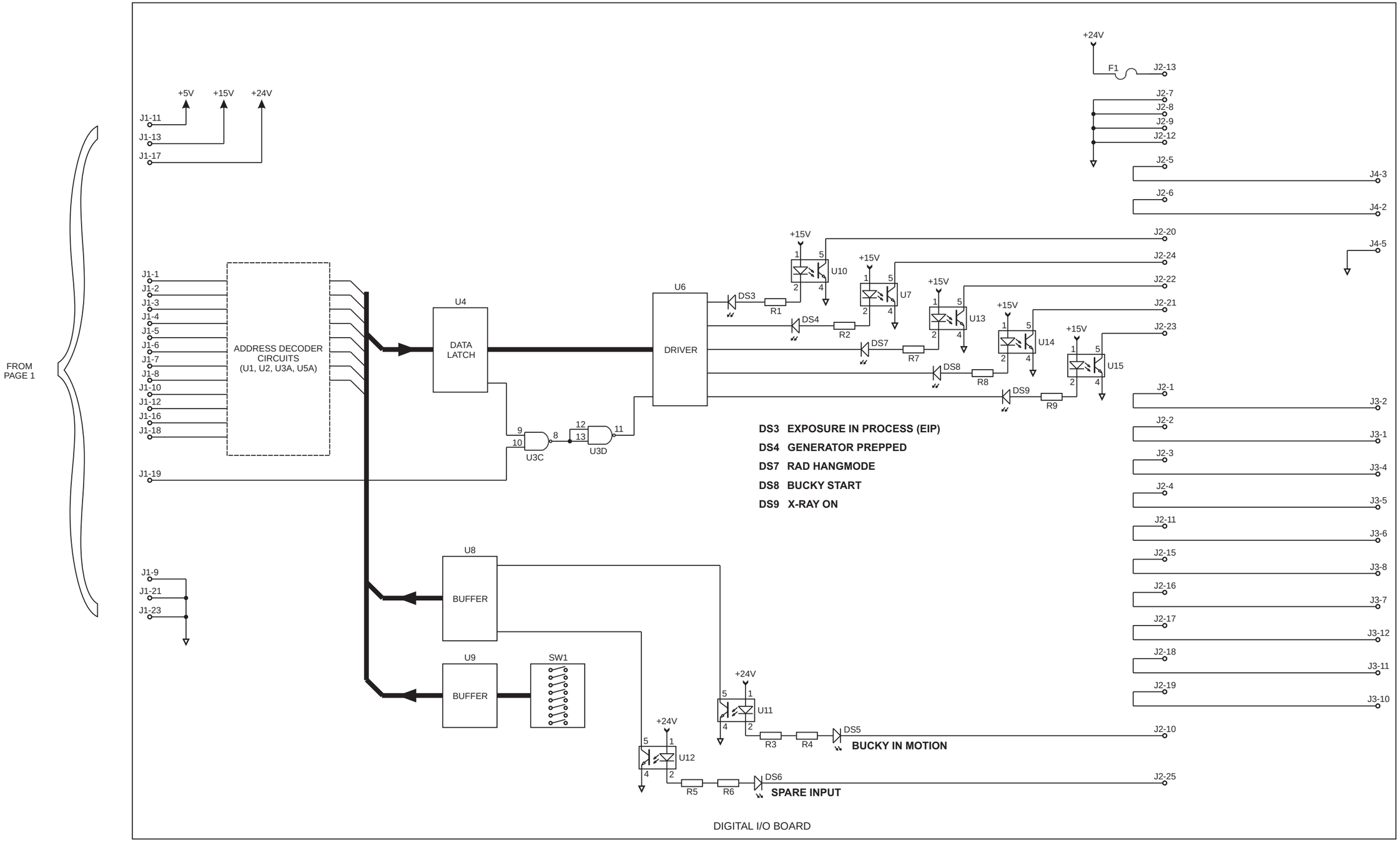

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 736153

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING THE CONNECTIONS TO J2, J3, J4.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 7 OF 19

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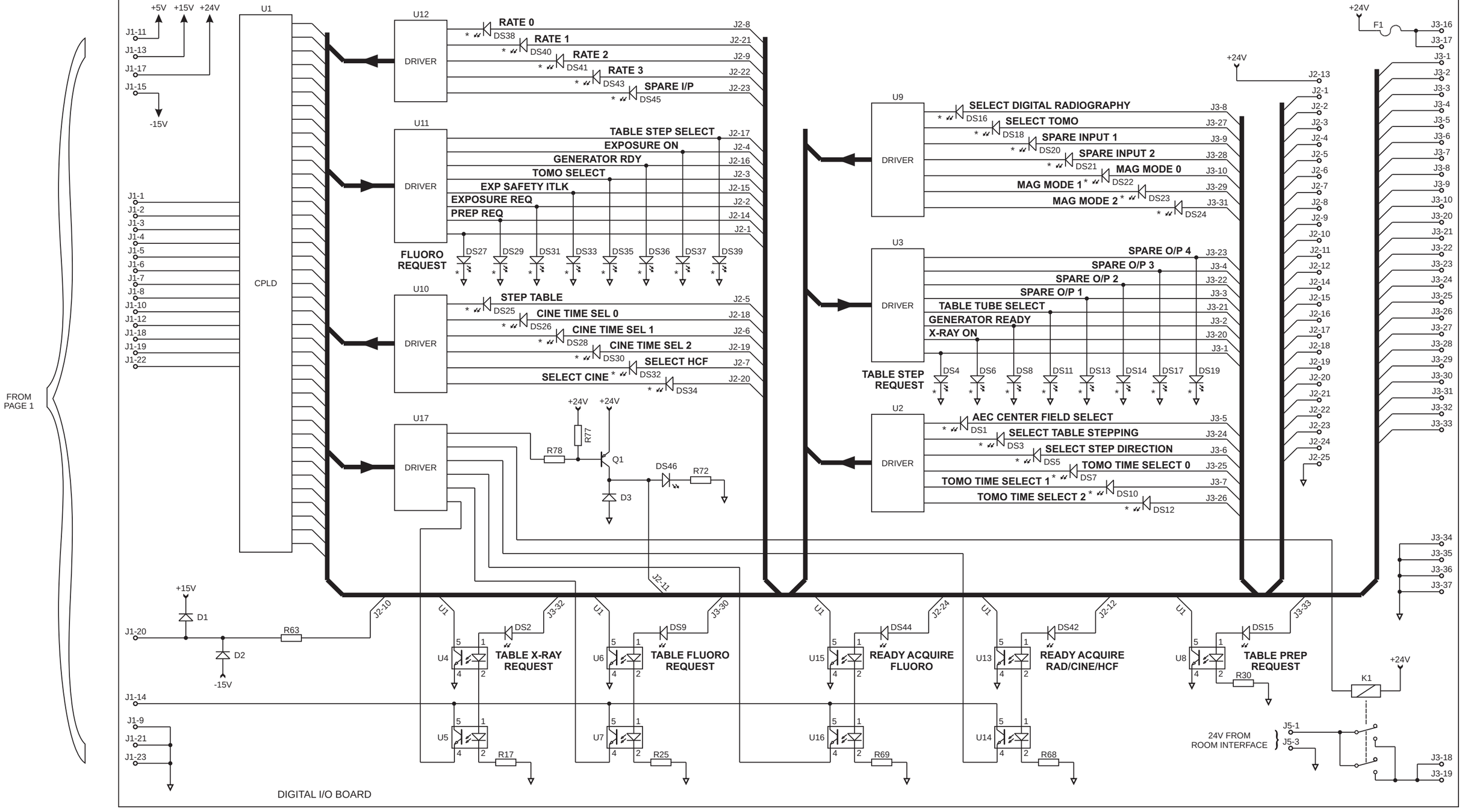

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 736894

* DUE TO SPACE RESTRICTIONS, SERIES RESISTORS ARE NOT SHOWN FOR THE INDICATED LED'S

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL
FOR DETAILS REGARDING THE CONNECTIONS TO J2, J3.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 8 OF 19

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FROM PAGE 1

+5V +15V +24V

J1-11
J1-13
J1-17

J1-19

U3D 12 13 11

U7 MONOSTABLE TIMER

U3B 4 5 6

U3C 9 10 8

+5V

DS1

XRAY ON

R10

U10 DRIVER 4 6 7

JW103 → **X-RAY ON** TO PAGE 10

J2-20 (-)
J2-19 (+)

+15V

J7-2
J7-3
J7-1
J7-4
J7-5
J7-7

+15V

J6-1
J6-2
J6-5
J6-14

J6-3
J6-4
J6-6
J6-7
J6-8

J1-1
J1-2
J1-3
J1-4
J1-5
J1-6
J1-7
J1-8
J1-10
J1-12
J1-16
J1-18

ADDRESS DECODER CIRCUITS (U1, U2, U3A, U5)

U17 DATA LATCH

U18 DRIVER

JW101 → **X-RAY RQST** TO PAGE 10

U4 DATA LATCH

U13 DRIVER 4 6 7

J2-17 (+)
J2-18 (-)

U11 DRIVER 4 6 7

J2-13 (+)
J2-14 (-)

R8
R6

XRAY DS4

DS2 **PREP**

U12 DRIVER 4 6 7

J2-15 (+)
J2-16 (-)

U6 DATA LATCH

U14 DRIVER 4 6 7

J2-21 (+)
J2-22 (-)

R7
R9

GENRDY DS3

DS5 *

J1-9
J1-21
J1-23

U8 BUFFER

U15 DRIVER 1 6 7

R4

J2-1 (+)
J2-2 (-)

U9 BUFFER

SW1

R5

DS6 *

+5V

DS7

XRAYEN

R12

+5V

R11

Q1

U16

5 1 4 2

J2-25 (+)
J2-26 (-)

JW102 → **X-RAY EN** FROM PAGE 10

J4-10
J6-9
J4-11
J6-10
J4-7
J6-11
J4-8
J6-12
J4-12
J6-13
J4-3
J4-9

J4-1
J5-3
J4-2
J5-7
J4-4
J5-2
J4-5
J5-8
J5-5

* THE INPUTS / OUTPUTS MARKED "*" ARE SPARE, AND HAVE NOT BEEN ASSIGNED

DIGITAL I/O BOARD

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 737950.
THIS SHOWS THE CONNECTIONS TO J2, J4, J5, J6 AND J7. THE REMAINING CIRCUITS ARE SHOWN ON THE NEXT PAGE.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING THE CONNECTIONS TO J2, J4, J5, J6, AND J7.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 9 OF 19

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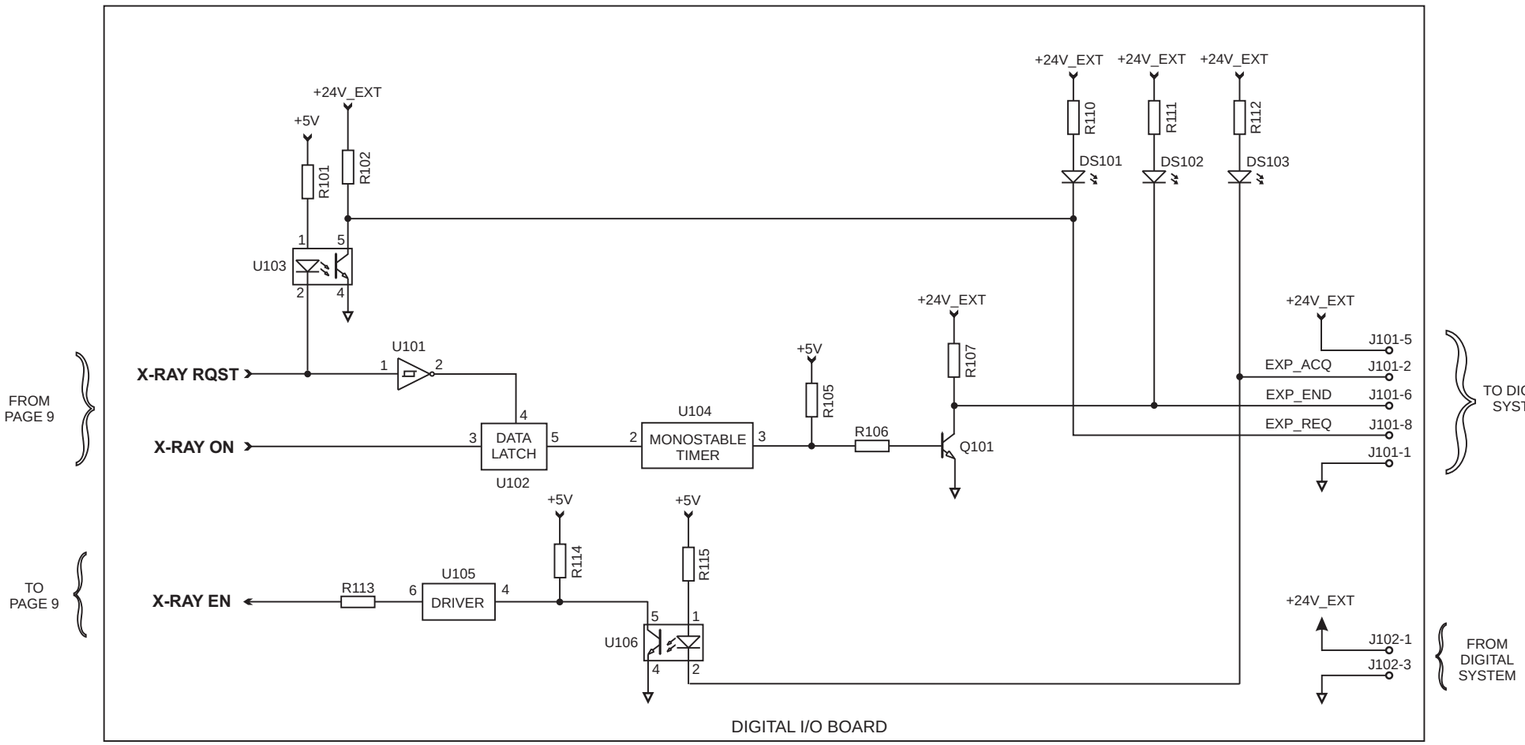
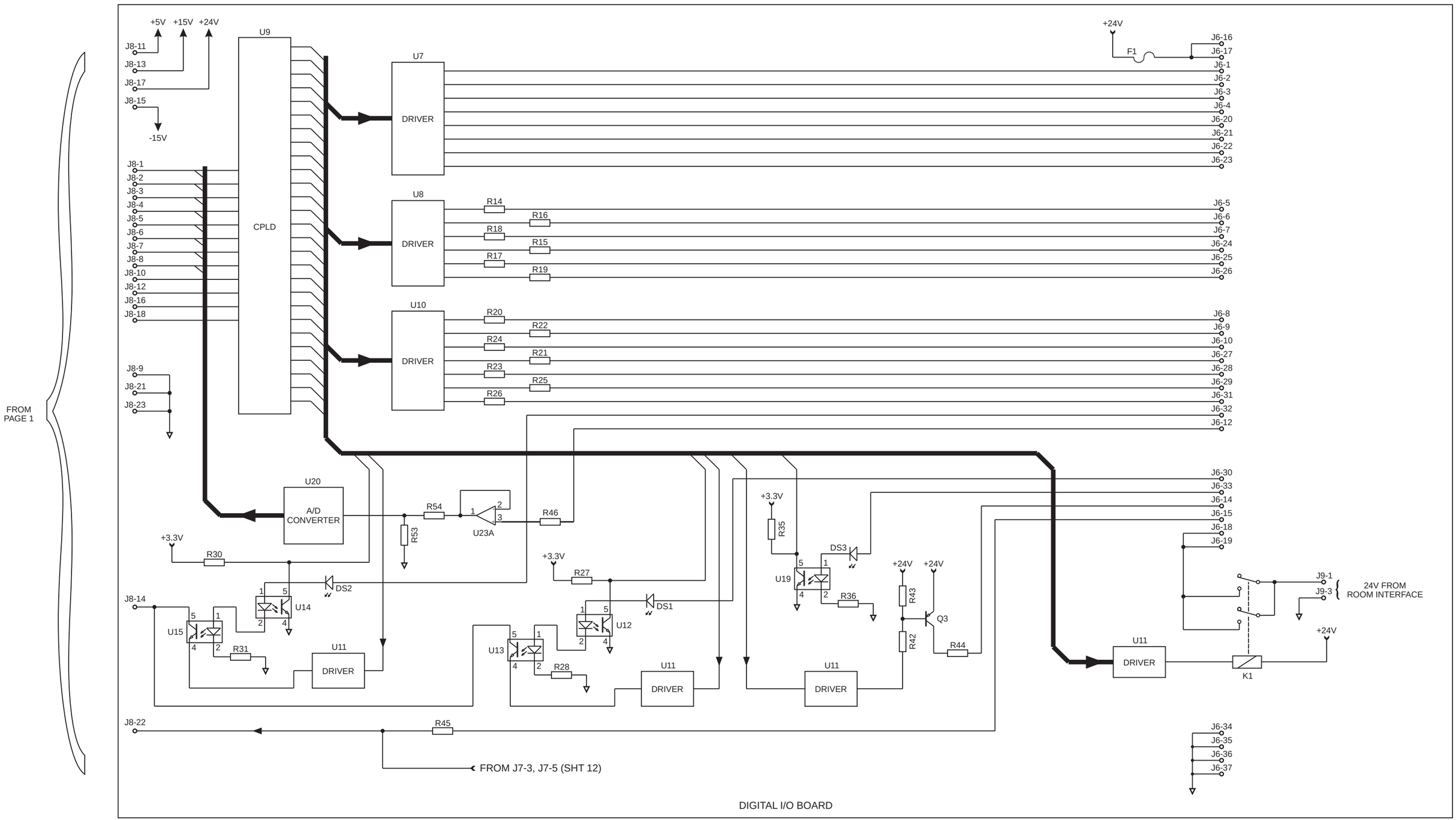


THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 737950. THIS SHOWS THE CONNECTIONS TO J101 AND J102. THE REMAINING CIRCUITS ARE SHOWN ON THE PREVIOUS PAGE.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING THE CONNECTIONS J101 AND J102.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 10 OF 19



THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 738947. THIS SHOWS THE CONNECTIONS TO J6 AND J9; THE REMAINING CIRCUITS ARE SHOWN ON THE NEXT PAGE.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING THE CONNECTIONS TO J6, J9.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 11 OF 19

Use and disclosure is subject to the restrictions on the title page of this CPI document.

FROM PAGE 1

U16
3.3V REGULATOR
+3.3V
+2.5V
J8-11
R8
U22
VOLTAGE REGULATOR
+10V
U21
VOLTAGE REGULATOR
J8-13
R49
R48
R47
U9
CPLD
J8-1
J8-2
J8-3
J8-4
J8-5
J8-6
J8-7
J8-8
J8-10
J8-12
J8-16
J8-18
U6
DRIVER
+24V
J4A-1
J4A-2
J4A-3
J4A-4
J4A-5
J4A-6
J4A-7
J4A-8
J4B-1
J4B-2
J4B-3
J4B-4
J4B-5
J4B-6
J4B-7
J4B-8
U5
DRIVER
J4C-1
J4C-2
J4C-3
J4C-4
J4C-5
J4C-6
J4C-7
J4C-8
J4D-1
J4D-2
J4D-3
J4D-4
J4D-5
J4D-6
J4D-7
J4D-8
U4
DRIVER
J4E-1
J4E-2
J4E-3
J4E-4
J4E-5
J4E-6
J4E-7
J4E-8
J4F-1
J4F-2
J4F-3
J4F-4
J4F-5
J4F-6
J4F-7
J4F-8
U3
DRIVER
J4G-1
J4G-2
J4G-3
J4G-4
J4G-5
J4G-6
J4G-7
J4G-8
J4H-1
J4H-2
J4H-3
J4H-4
J4H-5
J4H-6
J4H-7
J4H-8
U2
DRIVER
R6
R5
R4
J2-1
J2-2
J2-3
J2-4
J2-5
J2-6
R9
R7
J3-1
J3-2
J3-3
J3-4
J3-5
J3-6
J11-2
J11-1
U1
DRIVER
R3
R2
R1
J1-1
J1-2
J1-3
J1-4
J1-5
J1-6
R50
R51
R52
J10-1
J10-2
J10-3
J10-4
J10-5
J10-6
R12
R13
R10
R11
Q2
Q1
U11
DRIVER
R37
R38
R39
R40
Q4
Q5
J7-6
J7-4
J7-1
J7-3
J7-5
J7-2
D2
D1
U18B
U17
MONOSTABLE TIMER
J8-19
J8-20
R41
D3
D4
TO J8-22 (SHT 11)

DIGITAL I/O BOARD

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 738947. THIS SHOWS THE CONNECTIONS TO J1 TO J4, J7, J10, J11, AND THE VOLTAGE REGULATOR CIRCUITS; THE REMAINING CIRCUITS ARE SHOWN ON THE PREVIOUS PAGE.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING THE CONNECTIONS TO J1-J4, J7, AND J10.

DRAWN G. SANWALD	DATE 16 MAY 2000	DIGITAL INTERFACE
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	MD-0767 REV M
		SHEET 12 OF 19

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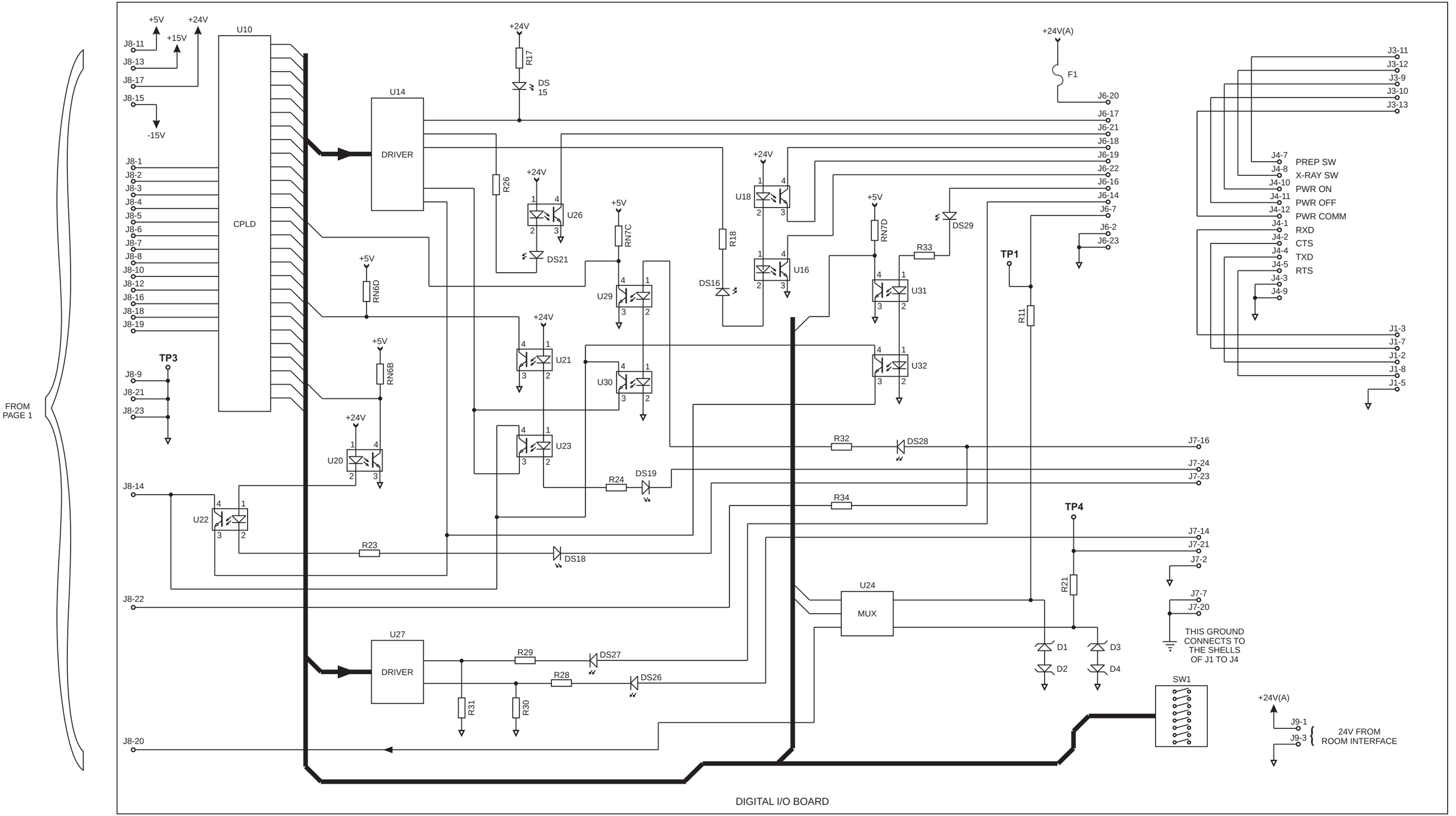


DIGITAL I/O BOARD

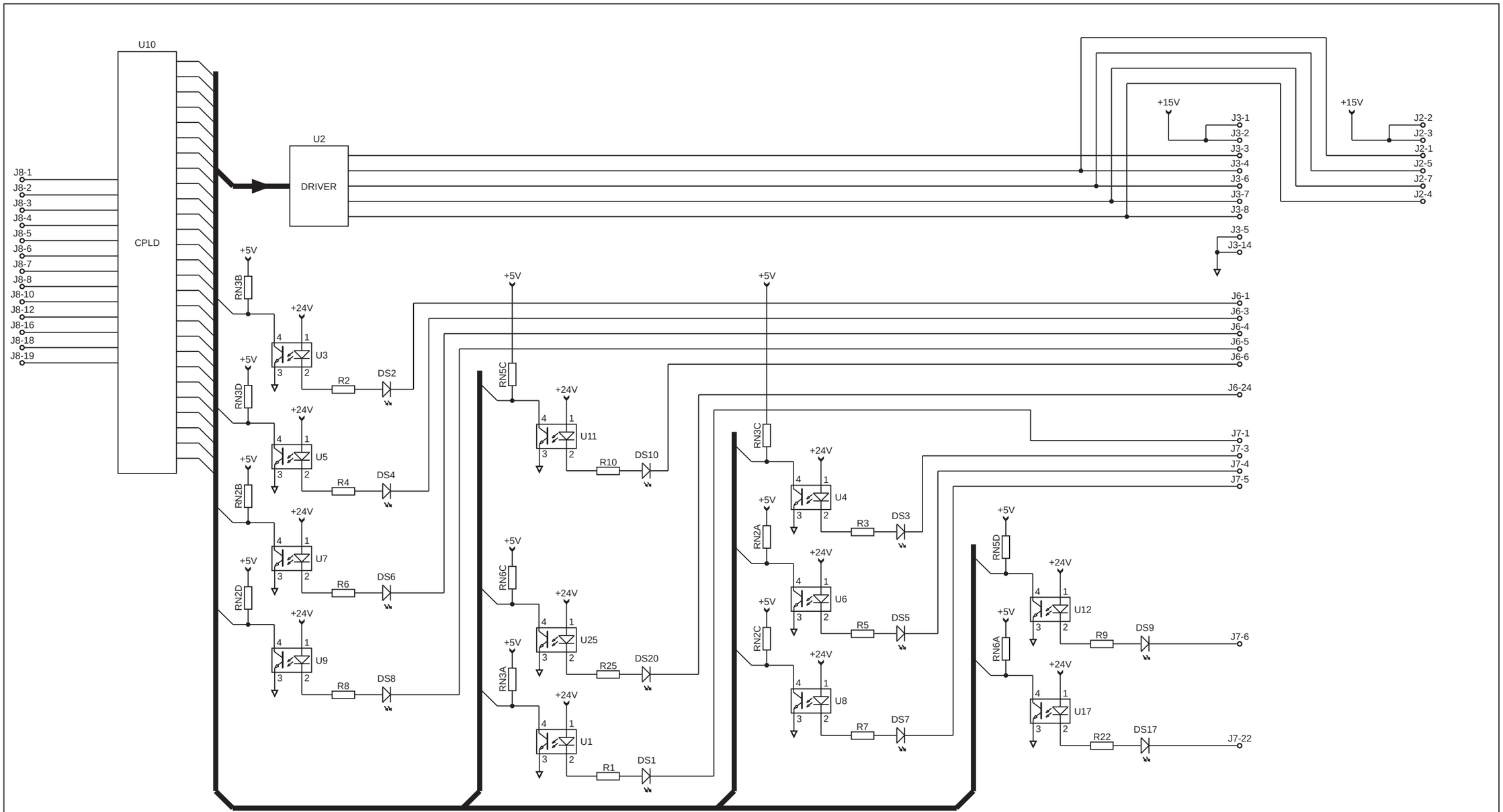
THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 738114. THE CIRCUITS FOR THIS BOARD ARE SPLIT BETWEEN SHEETS 13, 14, AND 15.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING THE CONNECTIONS TO J1, J2, J3, J4, J6, AND J7.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 13 OF 19

Use and disclosure is subject to the restrictions on the title page of this CPI document.

FROM PAGE 1



DIGITAL I/O BOARD

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 738114. THE CIRCUITS FOR THIS BOARD ARE SPLIT BETWEEN SHEETS 13, 14, AND 15.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL
FOR DETAILS REGARDING THE CONNECTIONS TO J1, J2, J3, J4, J6, AND J7.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 14 OF 19

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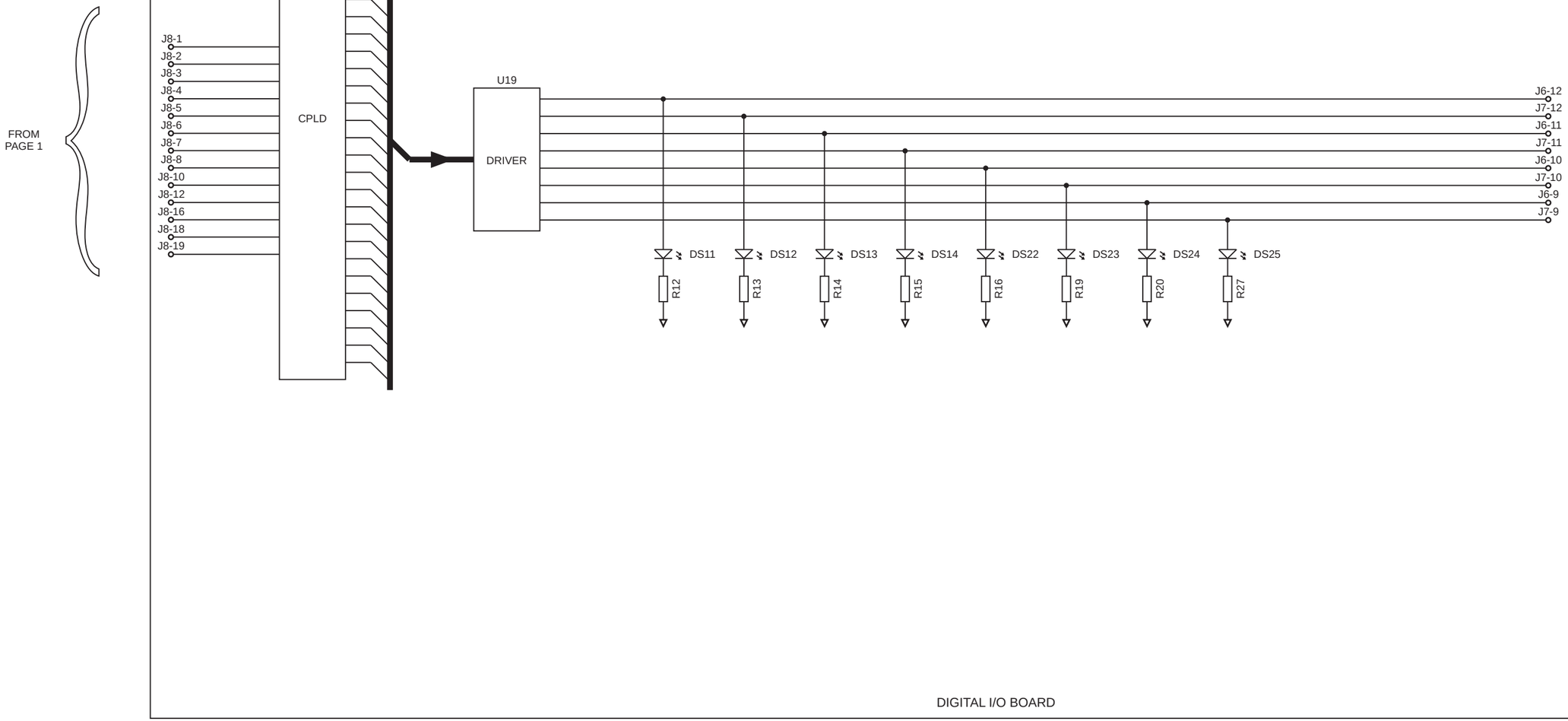

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 738114. THE CIRCUITS FOR THIS BOARD ARE SPLIT BETWEEN SHEETS 13, 14, AND 15.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL
FOR DETAILS REGARDING THE CONNECTIONS TO J1, J2, J3, J4, J6, AND J7.

DRAWN G. SANWALD	DATE 16 MAY 2000	DIGITAL INTERFACE
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	MD-0767 REV M
		SHEET 15 OF 19

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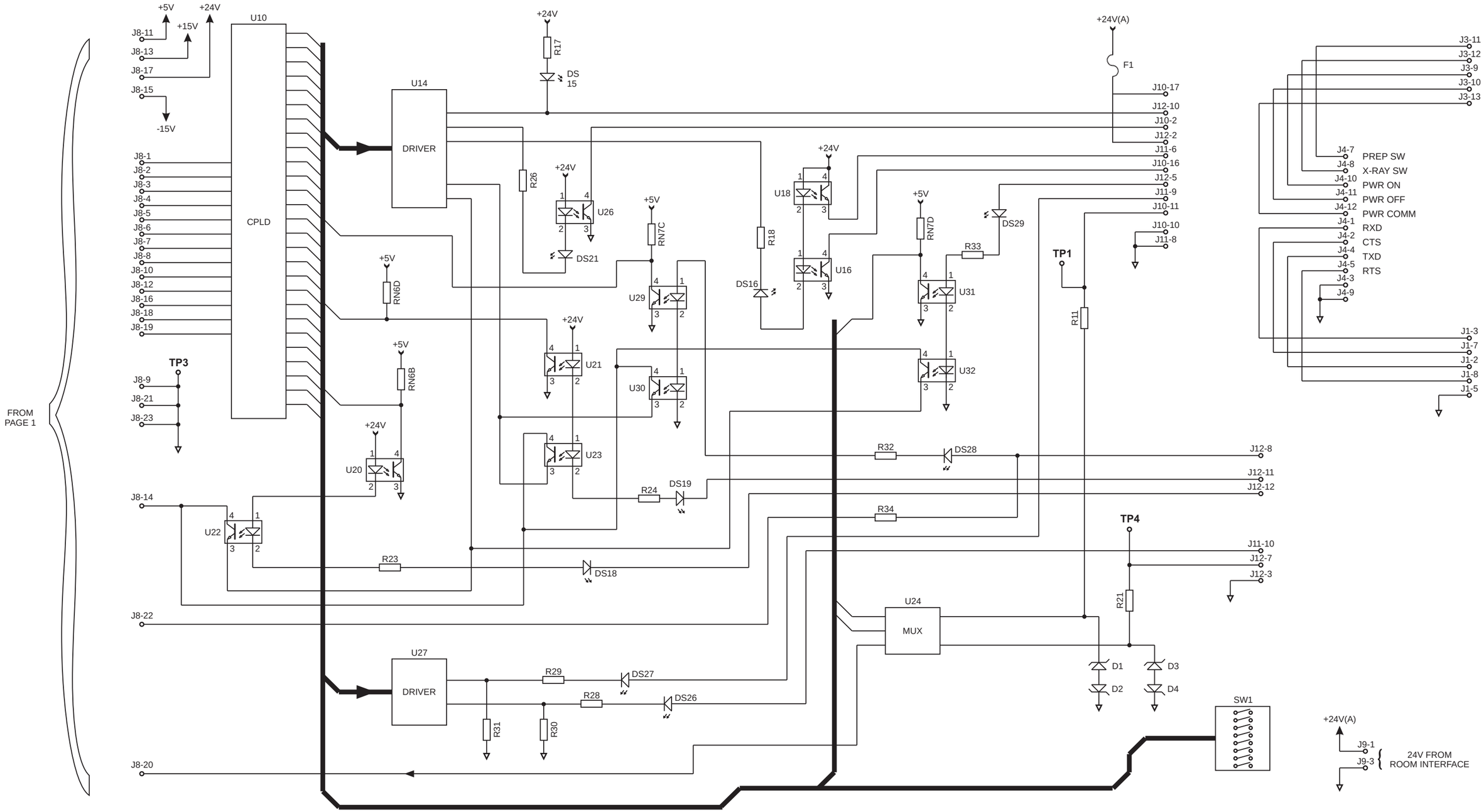


DIGITAL I/O BOARD

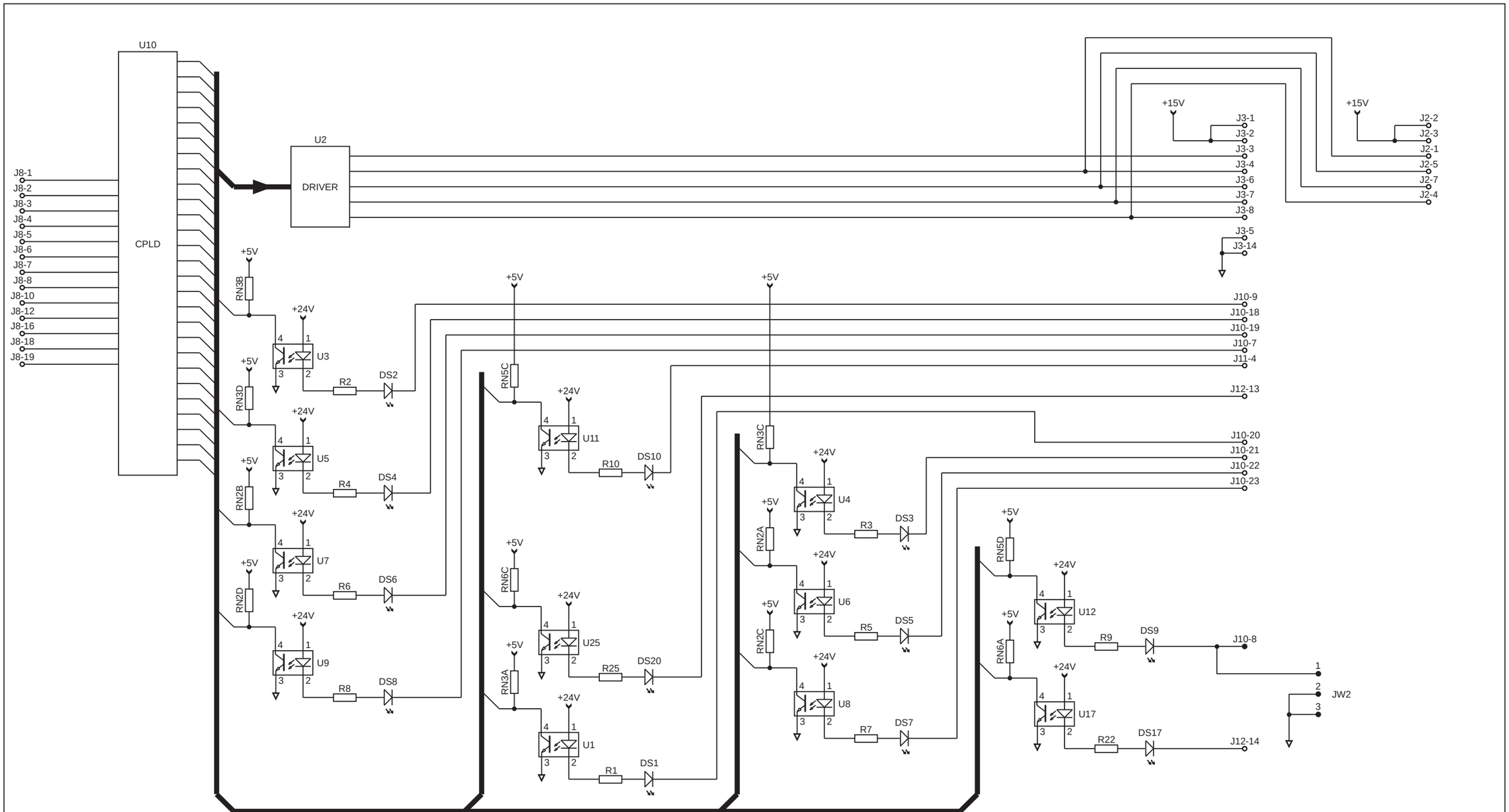
THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 902724. THE CIRCUITS FOR THIS BOARD ARE SPLIT BETWEEN SHEETS 16, 17, AND 18.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL
FOR DETAILS REGARDING THE CONNECTIONS TO J1, J2, J3, J4, J10, J11, J12, J13 AND J14.

DRAWN G. SANWALD	DATE 16 MAY 2000	DIGITAL INTERFACE
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	MD-0767 REV M
		SHEET 16 OF 19

Use and disclosure is subject to the restrictions on the title page of this CPI document.

FROM PAGE 1



DIGITAL I/O BOARD

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 902724. THE CIRCUITS FOR THIS BOARD ARE SPLIT BETWEEN SHEETS 16, 17, AND 18.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL
FOR DETAILS REGARDING THE CONNECTIONS TO J1, J2, J3, J4, J10, J11, J12, J13 AND J14.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 17 OF 19

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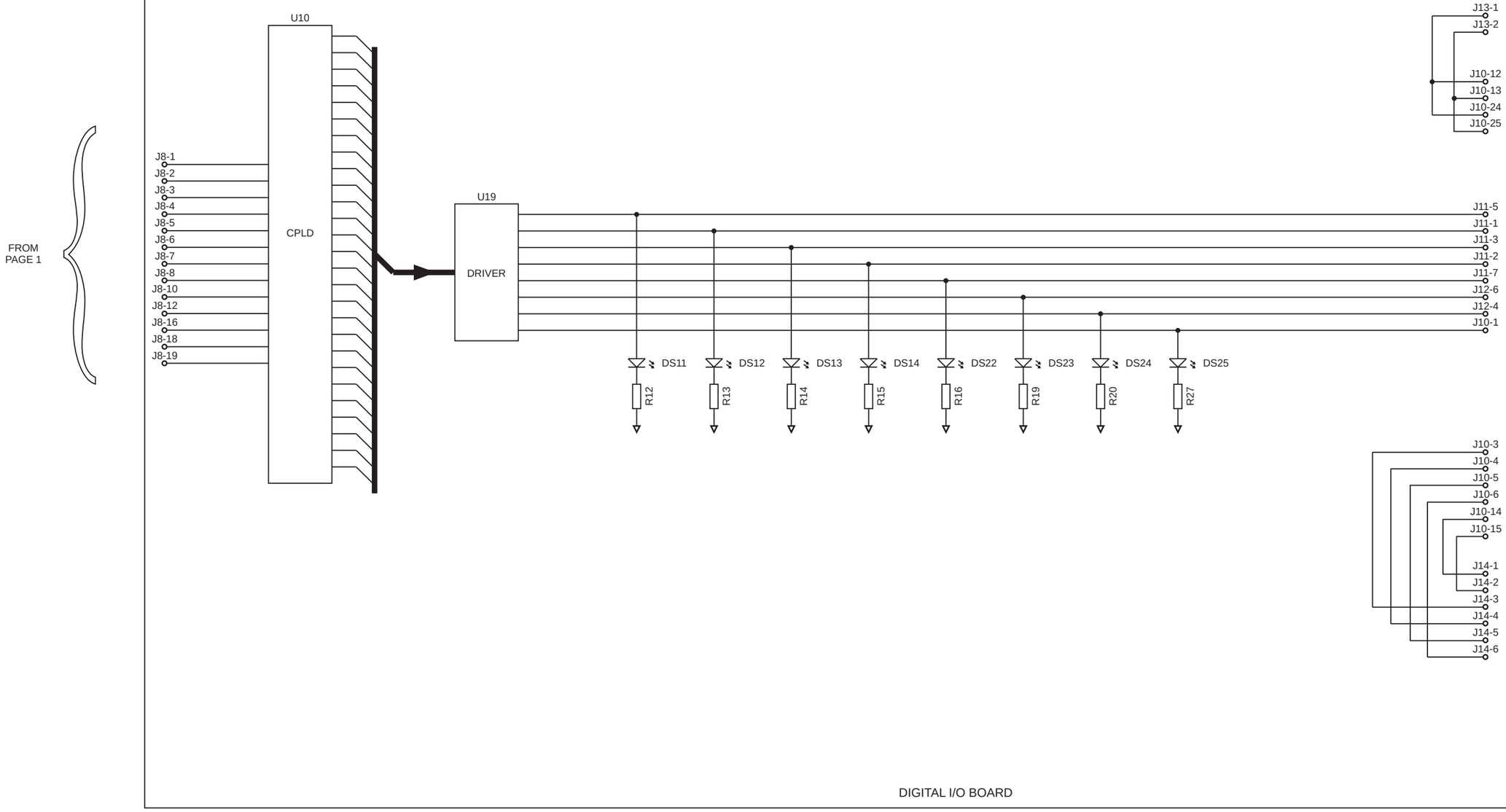

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 902724. THE CIRCUITS FOR THIS BOARD ARE SPLIT BETWEEN SHEETS 16, 17, AND 18.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL
FOR DETAILS REGARDING THE CONNECTIONS TO J1, J2, J3, J4, J10, J11, J12, J13 AND J14.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 18 OF 19

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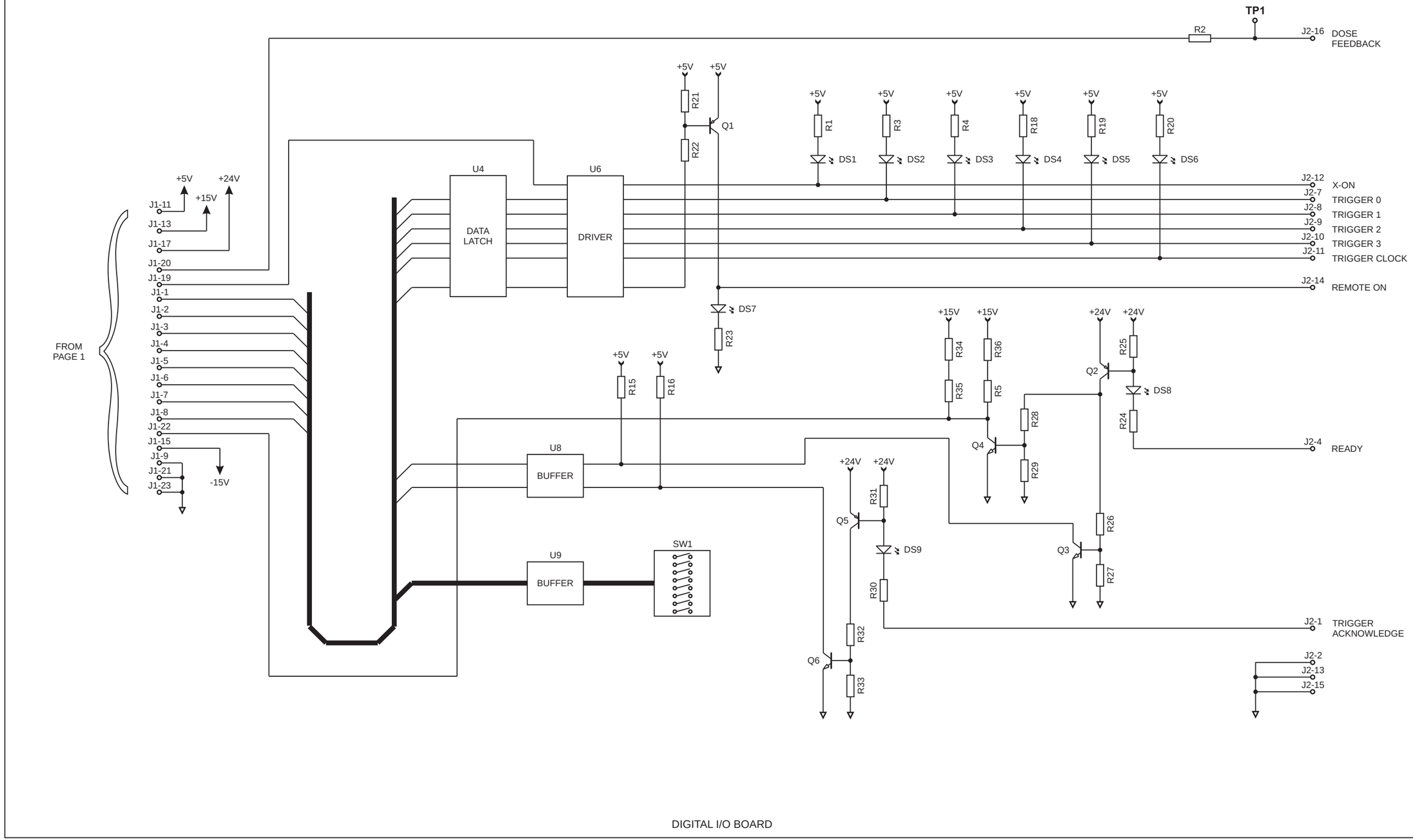

DIGITAL I/O BOARD

THIS SHEET APPLIES TO DIGITAL I/O BOARD ASSEMBLY 903121.

REFER TO THE DIGITAL IMAGING SUPPLEMENT IN THE SERVICE MANUAL FOR DETAILS REGARDING CONNECTIONS TO THIS BOARD.

DRAWN G. SANWALD	DATE 16 MAY 2000	**DIGITAL INTERFACE**
CHECKED KVR	17 MAY 2000	
DES.\MFG.\AUTH. L. FOSKIN	17 MAY 2000	**MD-0767 REV M**
		SHEET 19 OF 19

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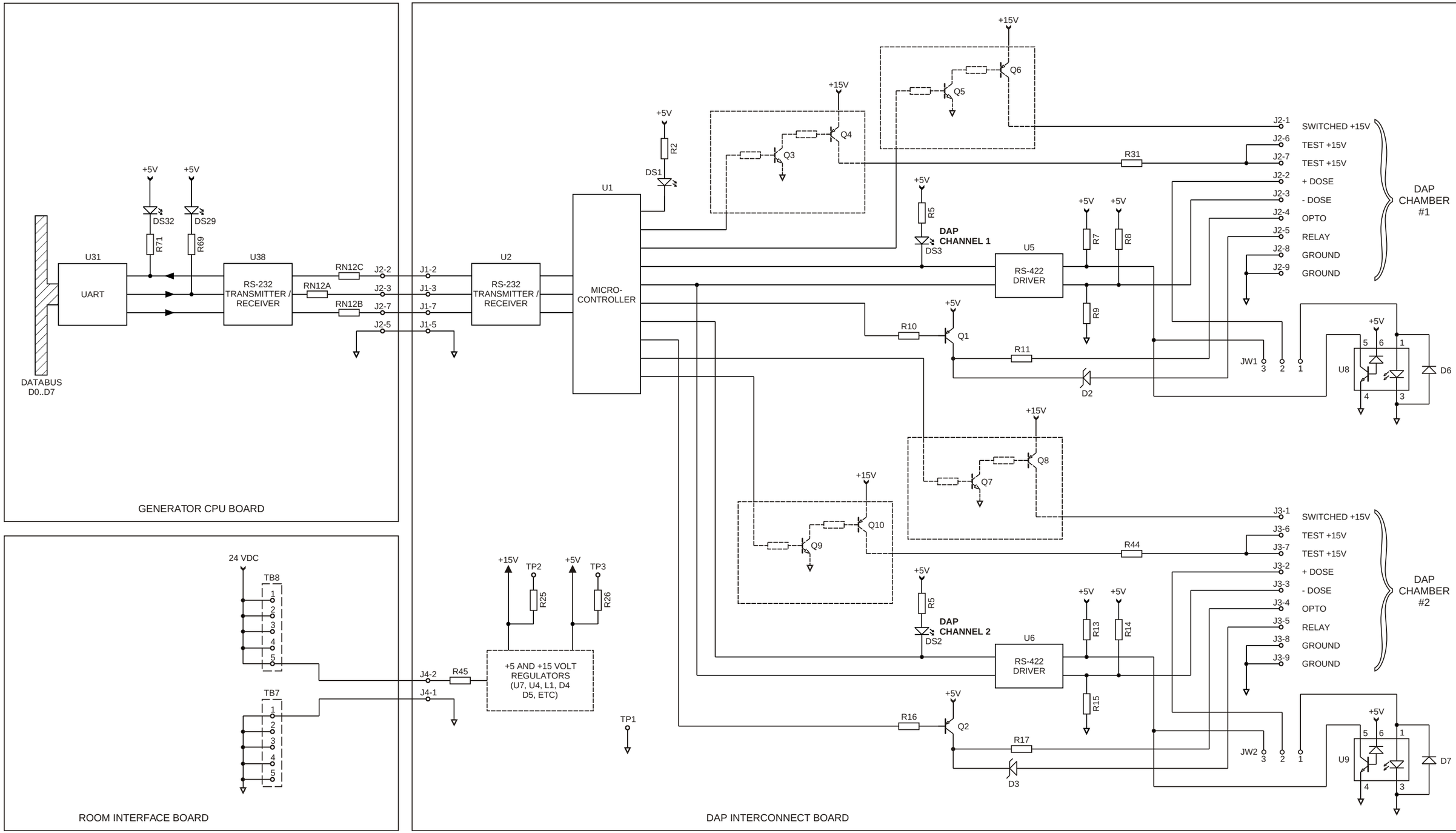

DRAWN G. SANWALD	DATE 16 JULY 2001	DAP
CHECKED M. LODER	21 AUG 2001	
DES.\MFG.\AUTH. L. FOSKIN	28 AUG 2001	MD-0828 REV D
		SHEET 1 OF 1

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CONSOLE BOARD (INDICO 100)

THIS SHEET SHOWS THE CONSOLE BOARD FOR INDICO 100 GENERATORS WITH THE 31 X 42 CM CONSOLE. REFER TO PAGE 2 FOR INDICO 100 GENERATORS WITH THE 23 X 56 CM CONSOLE AND THE RAD-ONLY CONSOLE.

CONSOLE CABLE

FROM RAD-ONLY CONSOLE (PAGE 2)

ALTERNATE CONSOLE CONNECTIONS

GENERATOR INTERFACE BOARD

GENERATOR CPU BOARD

* FOR RS-232: U1, U2, AND R16 ARE NOT FITTED.
FOR RS-422: U12, RN3C, RN3D, RN3A, AND RN3B ARE NOT FITTED.

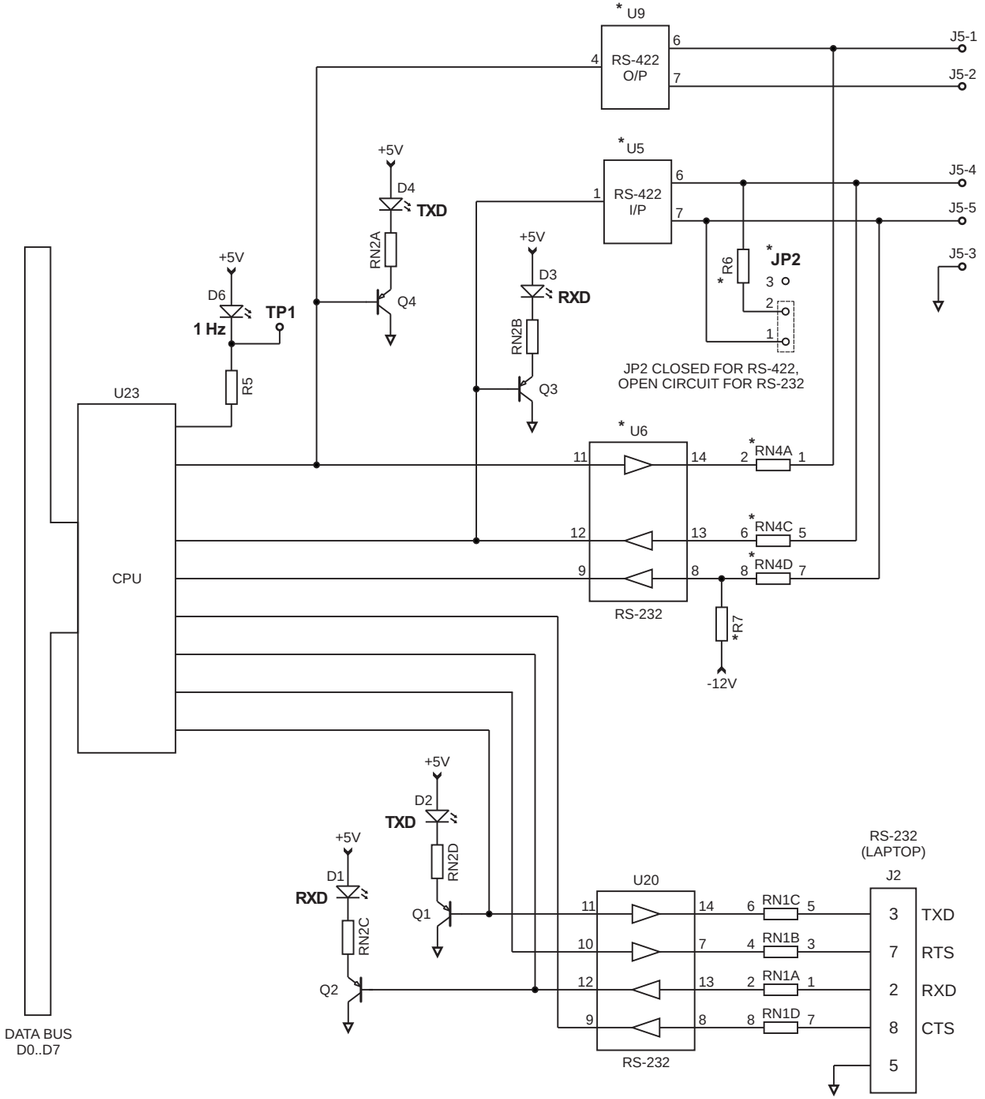
OPTIONAL COMMUNICATIONS PORTS ARE SHOWN ON PAGE 2

SERIAL PORT FOR REMOTE FLUORO CONTROL. REFER TO MD-0766

DRAWN G. SANWALD	DATE 13 DEC 2001	SERIAL COMMUNICATIONS
CHECKED J. BARNES	9 JAN 2002	
DES.\MFG.\AUTH. L. FOSKIN	9 JAN 2002	MD-0829 REV G
		SHEET 1 OF 2

Use and disclosure is subject to the restrictions on the title page of this CPI document.

*
FOR RS-232: U5, U9, JP2, AND R6 ARE NOT FITTED.
FOR RS-422: U6, RN4A, RN4C, RN4D AND R7 ARE NOT FITTED.

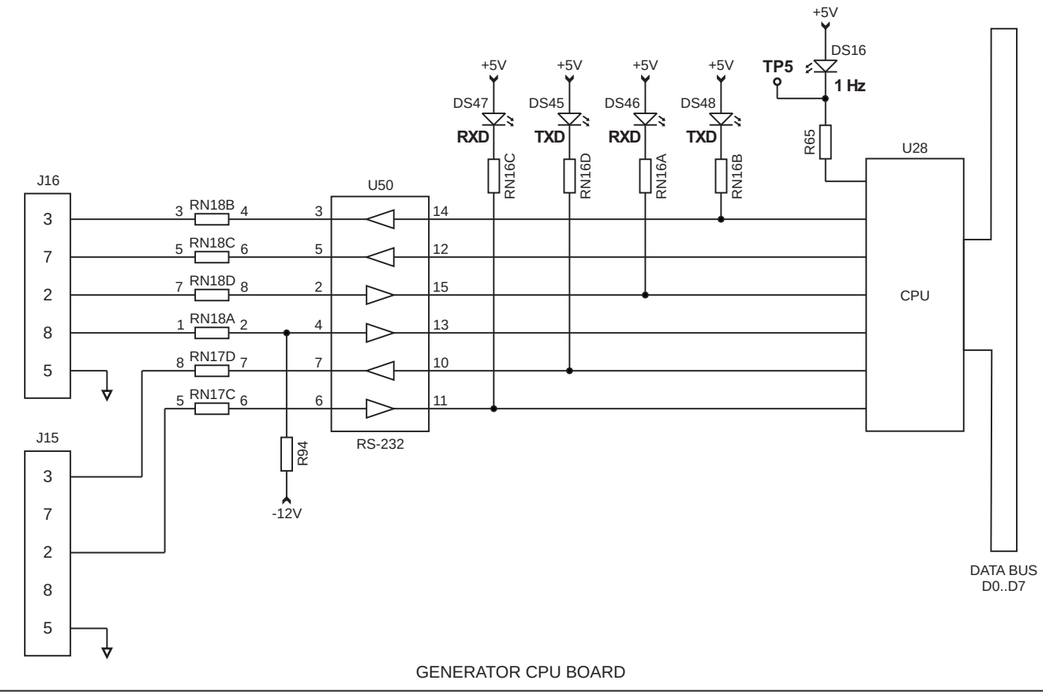


THIS AREA SHOWS THE CONSOLE CPU BOARD FOR INDICO 100 GENERATORS WITH THE 23 X 56 CM CONSOLE.

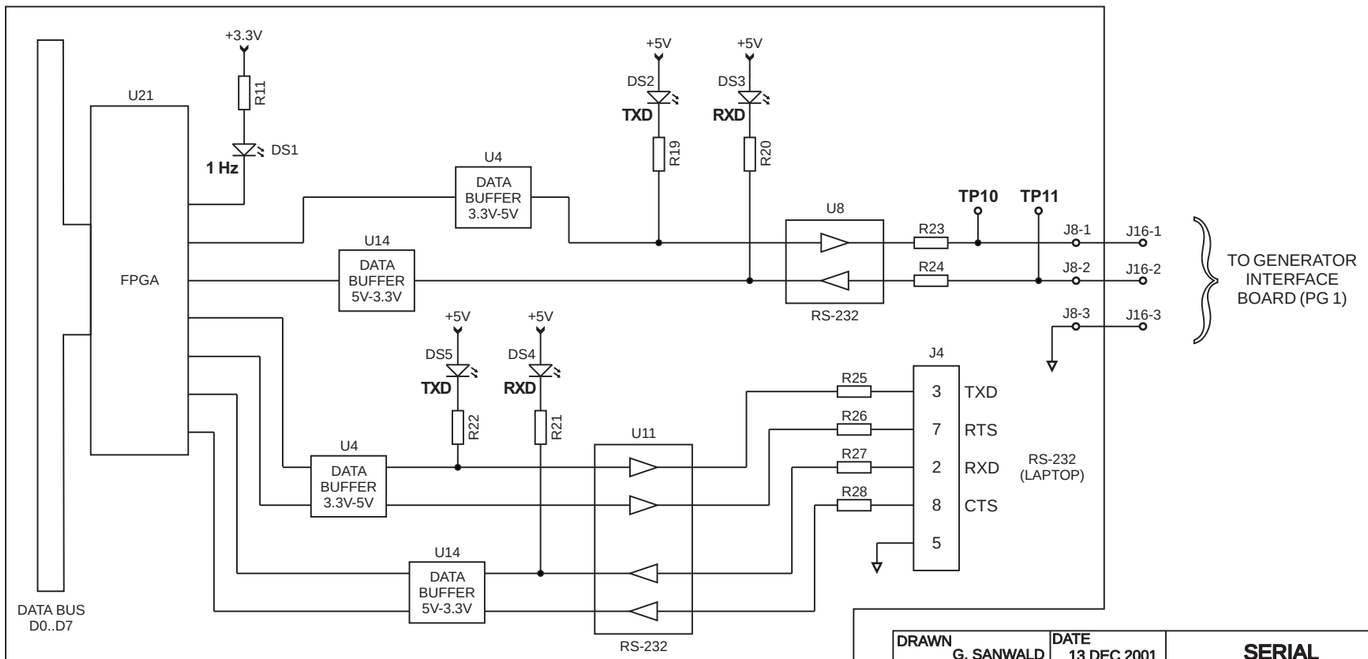
CONSOLE BOARD (INDICO 100)

TO GENERATOR INTERFACE BOARD (PG 1)

COMMUNICATIONS PORTS SHOWN BELOW ARE OPTIONAL



GENERATOR CPU BOARD



THIS AREA SHOWS THE CONSOLE CPU BOARD FOR INDICO 100 GENERATORS WITH RAD-ONLY CONSOLE.

CONSOLE BOARD (INDICO 100)

DRAWN G. SANWALD	DATE 13 DEC 2001	**SERIAL COMMUNICATIONS**
CHECKED J. BARNES	9 JAN 2002	
DES.\MFG.\AUTH. L. FOSKIN	9 JAN 2002	**MD-0829 REV G**
		SHEET 2 OF 2

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